ORIGINAL RESEARCH PAPER
Volume-6 | Issue-10 | October-2017 | ISSN No 2277 - 8179 | IF : 4.176 | IC Value : 78.46
INTERNATIONAL JOURNAL OF SCIENTIFIC RESEARCH

DESIGN AND ANALYSIS OF A SRAM CELL USING PULSED LATCH CIRCUIT

Engineering

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ABSTRACT

This paper describes a low power and delay effective SRAM (Static Random Access Memory) cell using pulsed latch circuit. The pulsed latch circuit consist of two cross coupled inverters and three NMOS transistors. In the proposed design, two access transistors present in the basic 6T SRAM cell are replaced by the pulsed latch circuit. The conventional and proposed SRAM cell, both the cells are designed in 65nm and 130nm CMOS technology with 1.0V and 1.5V power supply in Tanner tool v16.0. In comparison with the conventional SRAM cell, the proposed design yields better results in terms of power and speed. In the proposed design delay reduces drastically as compared to that of the conventional SRAM cell.

KEYWORDS

SRAM cell, Pulsed latch circuit, Power, Delay, NMOS transistors, CMOS technology and Tanner tool.

INTRODUCTION

SRAM has become a major component in many VLSI chips due to their large storage density, high operating speed, lower power dissipation and small access time. SRAM has become the topic of research due to its increase demand for laptops, mobiles, IC memory cards etc. The portable devices are gaining more popularity as well as making changes in every aspect of our daily lives. They are widely used for mobile applications for both on-chip and off-chip memories. There is a huge requirement of SRAM device in the field of multimedia data processing, which includes the image/video applications. Video applications require a large amount of embedded memory, which results in significant power consumption and also require high speed for which there should be less delay. Due to explosive growth of battery operated appliances, increased integration and operating speed it is very necessary to reduce power dissipation and delay[1]-[7].

The standard SRAM cell consist of 6T transistors. The SRAM (Static Random Access Memory) is a type of memory that uses bistable latching circuitry to store binary logic '1' or '0' bits. The standard SRAM cell consist of two cross-coupled inverter which act as a storage device and two NMOS access transistors which act as a switch and connecting these inverters to bit lines. The design of a standard 6T SRAM cell is shown in Figure 1.

This paper proposes a low-power and delay-effective SRAM cell using pulsed latch circuit. The SSASPL (Static Differential Sense Amp Shared Pulse Latch), is the smallest latch which is implemented in this design. The schematic of the SSASPL is shown in Figure 2 [9]-[13].

The SSASPL consist of 7 transistors. It has three inputs and two output signals. It updates its data through two differential data inputs with pulsed clock signal. Also, it has two differential data outputs. When the pulsed clock signal is high then only data is updated. The value of pull-down current of the three NMOS transistors (M1-M3) must be larger than the value of pull-up current of the PMOS transistors in the inverters [14] - [17].

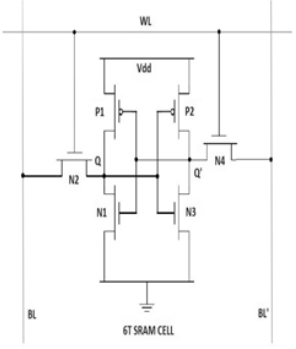


Figure 1: Schematic of a standard 6T SRAM cell

Sources: https://allthingsvlsi.wordpress.com

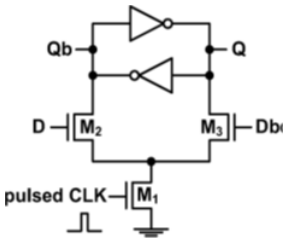


Figure 2: Schematic of the SSASPL [13]

Sources: IEEE Transactions on Circuits and Systems-I: Regular Papers

METHODOLOGY

In this paper we will design SRAM cell in standard form as well as using pulsed latch circuit in 65nm and 130nm CMOS technology. This design is carried out in Tanner tool v16.0.

A. A Standard 6T SRAM Cell in 65nm and 130nm Technology

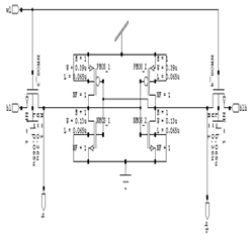


Figure 3: Schematic of a standard 6T SRAM cell in 65nm technology

Sources: Designed in Tanner tool v16.0 in S-Edit

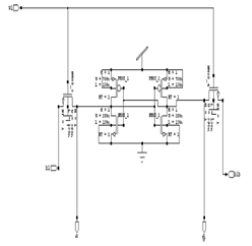


Figure 4: Schematic of a standard 6T SRAM cell in 130nm technology
Sources: Designed in Tanner tool v16.0 in S-Edit

The standard 6T SRAM cell consist of two PMOS transistors and four NMOS transistors . The two cross coupled inverters act as a storage device while the two NMOS access transistors act as a switch. The schematic of a standard 6T SRAM cell in 65nm and 130nm technology is shown in Figure 3 and 4 respectively.

B. SRAM Cell using Pulsed Latch Circuit in 65nm and 130nm Technology

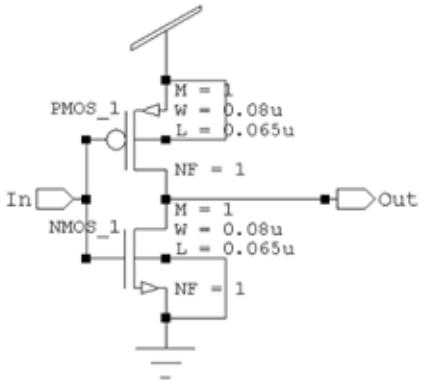


Figure 5: An Inverter circuit in 65nm technology
Sources: Designed in Tanner tool v16.0 in S-Edit

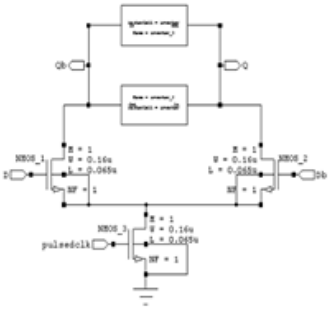


Figure 6: A Pulsed Latch circuit in 65nm technology
Sources: Designed in Tanner tool v16.0 in S-Edit

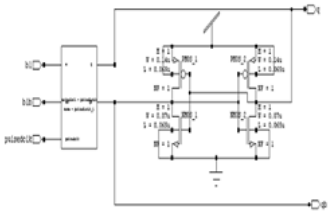


Figure 7: SRAM Cell using pulsed latch circuit in 65nm technology

Sources: Designed in Tanner tool v16.0 in S-Edit

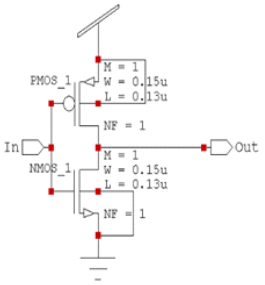


Figure 8: An Inverter circuit in 130nm technology

Sources: Designed in Tanner tool v16.0 in S-Edit

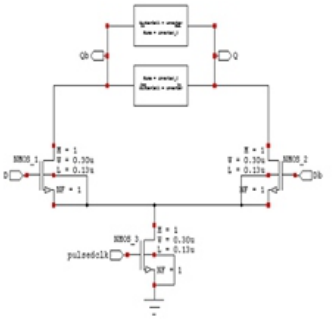


Figure 9: A Pulsed Latch circuit in 130nm technology
Sources: Designed in Tanner tool v16.0 in S-Edit

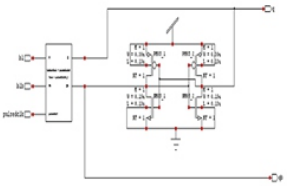


Figure 10: SRAM Cell using pulsed latch circuit in 130nm technology

Sources: Designed in Tanner tool v16.0 in S-Edit
We have designed SRAM cell using pulsed latch circuit in 65nm and 130nm CMOS technology with different w/l ratios and with 1.0V and 1.5V power supply. The design of SRAM cell using pulsed latch circuit in 65nm and 130nm technology is shown above in Figure 7 and Figure 10 respectively. Also, their sub-circuits are shown in Figure 5, 6, 8 and 9 respectively.

RESULTS AND DISCUSSIONS

A. Waveforms

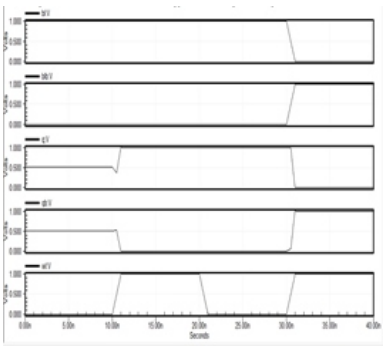


Figure 11: Waveform of a 1bit Standard 6T SRAM Cell in 65nm technology

Sources: Simulated in Tanner tool v16.0 in W-Edit

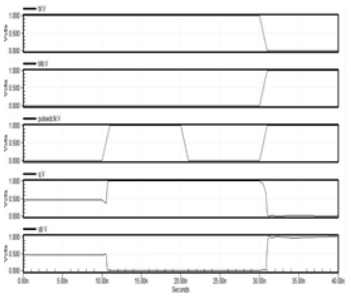


Figure 12: Waveform of a 1bit SRAM Cell using Pulsed Latch Circuit in 65nm technology

Sources: Simulated in Tanner tool v16.0 in W-Edit

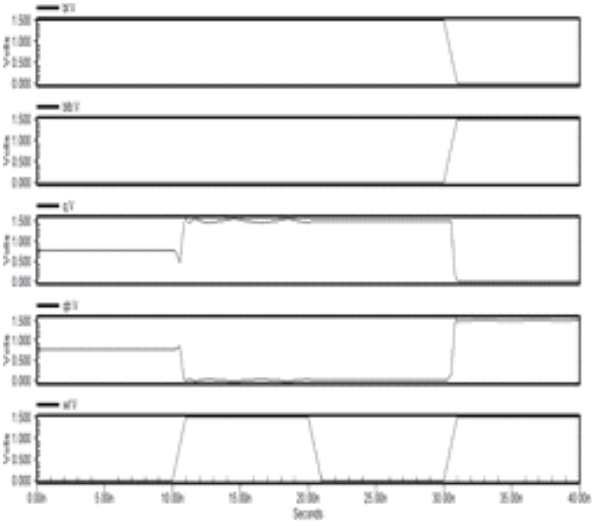


Figure 13: Waveform of a 1bit Standard 6T SRAM Cell in 130nm technology

Sources: Simulated in Tanner tool v16.0 in W-Edit

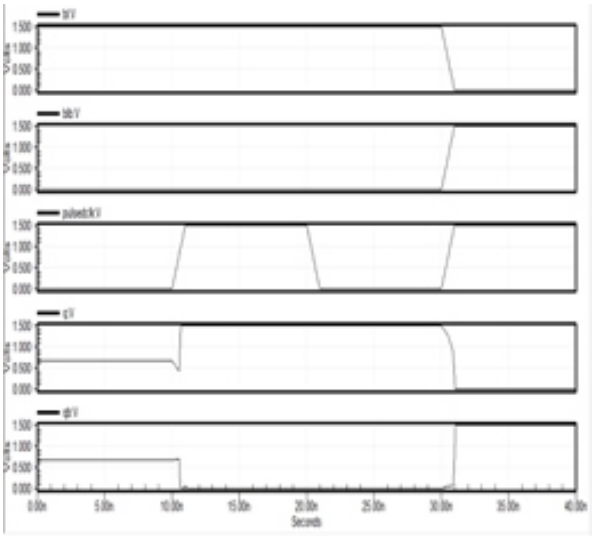


Figure 14: Waveform of a1bit SRAM Cell using Pulsed Latch Circuit in 130nm technology

Sources: Simulated in Tanner tool v16.0 in W-Edit

From the above figures we came to know that the waveforms obtained from both the methodologies are almost same .So we can say that our design approach is in the right path.

A. Simulation Results

We have seen that the waveforms of standard and proposed SRAM cell are almost same. Here we will compare the power requirement, delay and the total number of transistors required in the designing of 1bit SRAM cell in both the methodologies.

TABLE-1
SIMULATION RESULTS OF 1BIT SRAM CELL IN 65nm TECHNOLOGY

PARAMETERS	Standarad 6T SRAM Cell Design	Proposed SRAM Cell Design
Technology(nm)	65	65
No. of Transistors	6T	11T
Averagr Power (watts)	11.83435µ	9.164842µ
Average Delay (seconds)	99.7720p	82.5754p

Sources: Simulated in Tanner tool v16.0

TABLE 2

SIMULATION RESULTS OF 1BIT SRAM CELL IN 130nm TECHNOLOGY

PARAMETERS	Standard 6T SRAM Cell Design	Proposed SRAM Cell Design
Technology(nm)	130	130
No. of Transistors	6T	11T
Averagr Power (watts)	86.60393µ	71.78293µ
Average Delay (seconds)	141.1350p	90.8518p

Sources: Simulated in Tanner tool v16.0

CONCLUSIONS

In the previous section we have compared the standard and proposed SRAM cell design for 1bit, in 65nm and 130nm CMOS technology The results obtained are shown in Table-1 and Table-2. From the obtained results we can conclude that the proposed design gives better results in terms of power and delay. The main aim of the pulsed latch circuit is to reduce delay of the circuit. This design approach can be used for n number of bits which results in low power and reduce delay.

REFERENCES

[1] Agal, A., Pradeep, Krishnan, B., "6T SRAM Cell:Design And Analysis", International Journal of Engineering Research and Applications, 4(3) March 2014,pp. 574–577.

[2] Yadav, S., Malik, N. ,Gupta, A.and Rajput, S., " Low Power SRAM Design with Reduced Read/Write Time", International Journal of Information and Computation Technology, 3(3) 2013, pp. 195–200.

[3] Gopal, M.,Prasad, S.S.D. and Raj, B., "8T SRAM Cell Design for Dynamic and Leakage Power Reduction", International Journal of Computer Applications, 71(9) May 2013.

[4] Subudhi, T. and Mehra, R., " Design Analysis of CMOS Voltage Mode SRAM Cell using Different nm Technologies",International Journal of Emerging Technologies and Engineering, 1(3) April 2014.

[5] Sharma, R., Antil, R. and Kumar, K., "Comparitive Study of 6T and 8T SRAM Using Tanner Tool",International Journal of Computer Science and Mobile Computing.

[6] Apostolidis, G., Balobas, D. and Konofaos, N., "Design and simulation of 6T SRAM cell architectures in 32nm technology", PACET 2015.

[7] Kaur, N., Kaur, L. and Kaur, G., "Design and Performance Analysis of Low Power 6T SRAM Cell Using Tanner Tool",International Journal of Emerging Engineering Research and Technology, 3(4) April2015, pp16-21.

[8] Tejaswini, N., and Karunashree, B., "VLSI DESIGN OF NOVEL RAM USING PULSED LATCH BASED SHIFT REGISTERS", International Journal of Professional Engineering Studies, Volume VI, Issue 3,May 2016.

[9] Kumar , M.M.,and Sekhar, C.N., "Design and Analysis of Low Power Pulse Triggered Flipflop Based on Single Feed-Through Scheme", International Journal of Engineering Research,3(2),pp 47-51.

[10] Partovi, H.,et.al. "Flow – Through Latch and Edge Triggered Flip-Flop Hybrid Elements",IEEE, International Solid-State Circuits Conference, 1996.

[11] Stojanovic, V. and Oklobdzija, V.G. "Comparitive Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power Systems",IEEE Journal of Solis-State Circuits, 34 (4) April 1999.

[12] Heo, S., Krashinsk, R. and Asanovic, K., "Activity-Sensitive Flip-Flop and Latch Selection for Reduced Energy",ARVLSI, March 15,2001.

[13]Yang,D.B.,"Low-Power and Area-Efficient Shift Register Using Pulsed Latches",IEEE Transactions on Circuits and Systems-I:Regular Papers, 62(6) June 2015,pp 1564-1571.

[14] Tarkasvar, J., Pachori, K.and Jain, R. Dr., "Power and Area Optimization of Pulse Latch Shift Register",International Journal of Engineering Research and Development,12(6)June 2016, pp 41-45.

[15] The, C.K, Hamada, M., Hara, H. and Fujita, T., "A 77% energy-saving 22 transistor single-phase-clocking-D flip-flop with adaptive-coupling configuration in 40nm",IEEE,IEEE Xplore,7 April 2011.

[16] Kumar, R.,.Bollapalli,C.K, Garg, R., Soni, T. and Khatri, P.S., "A Robust Pulsed Flip-Flop and its use in Enhanced Scan Design",IEEE,2009.

[17] Kakde,D.S., Pokle, B.P. and Dorave, J., "Low Power VLSI design Methodologies & Power Management", International Journal of Research in Advent Technology, 4(4)April 2016, pp 277-281.