Volume : 5 | Issue : 10 | October 2016 • ISSN No 2277 - 8179 | IF : 3.508 | IC Value : 69.48

Positive Feedback Adiabatic Logic for Circuits of Higher Frequency and Lower Power

Engineering

KEYWORDS : Adiabatic Circuit, Energy recovery logic, Charge recovery logic, Positive Feedback Adiabatic Logic

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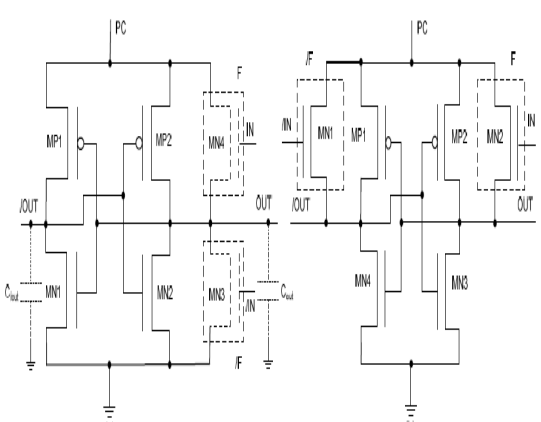
ABSTRACT

This paper presents the quasi-adiabatic Asymmetrical Positive Feedback Adiabatic Logic (APFAL) for low power operation through energy recovery technique. The topology of a logic gate defines the logic effort and it determines the gate sensitivity. The APFAL strives to reduce the logic effort of one arm of the 2N2P latch which results in reduced values of adiabatic and non-adiabatic power components. The use of asymmetric complementary functional blocks in the sense-amplifier structure achieves this. Furthermore, the APFAL incurs reduced transients and minimized floating node problems. It is a diode-free and dual rail logic offering both the true and complementary outputs. It achieves significant reduction in switched capacitance resulting in faster response. Efficient energy recovery is achieved for frequency range of up to 500 MHz. The need for reduced interconnects and realization of less leakage are the added advantages. Validation is done through full-custom designed arithmetic circuits. Comparison with static CMOS and PFAL circuits are made to validate the design. In post-layout simulations, the 8-bit APFAL multiplier achieves an adiabatic gain of 14.91 at 100 MHz to 6.45 at 500 MHz against the static CMOS counterpart. Energy savings of 27% and 22.5% are achieved against the optimized PFAL 4-bit CLA and 8- bit multiplier equivalent circuits respectively, at 500 MHz.

I. INTRODUCTION

An enormous amount of power is dissipated in high performance applications. Thus, the major deliberation needed in the design of VLSI circuits and systems, while using deep

submicron technologies is the design for low power. The focus of circuit design has been towards the search for innovative unconventional low power design techniques. The adiabatic or energy recovery design is a novel circuit design method envisaged in this direction, which operates with minimum power dissipation and tolerable circuit complexity [1]. They reclaim full or partial energy stored in the nodal capacitances and recycle them. They are classified into (1) fully adiabatic and (2) quasi-adiabatic circuits. While the former has no nonadiabatic loss realized at the expense of higher circuit density, the latter incurs some non-adiabatic loss with simpler circuit style. Navigating the current through devices with small potential difference and realizing efficient charge recovery from the nodal capacitances makes this possible. A number of quasi-adiabatic logic circuits consisting of the basic 2P or 2N2P latch operating at few hundreds of megahertz frequencies [2]-[5] and a gigahertz class Boost logic [6] have been presented. Of these, the Positive Feedback Adiabatic



Logic (PFAL) [5] exhibits the lowest power consumption.

II. ASYMMETRIC POSITIVE FEEDBACK ADIABATIC LOGIC (APFAL)

The APFAL uses the sense amplifier consisting of two PMOS devices MP1 and MP2, and two NMOS devices MN1 and MN2 as shown in Fig. 1(a). These four devices together form a 2N2P latch. The complementary functional blocks F and /F are connected in parallel with the PMOS and NMOS devices of the latch. The inverter/buffer circuit is powered by the power-clock (PC). The adiabatic pipeline is run by four 4-phase power-clocks each lagging behind the other by 90o as depicted in Fig. 2. The PFAL circuit is shown in Fig. 1(b) for comparison. The four phases of operation are (1) Evaluate, (2) Hold (3) Recover and (4) Wait. To elaborate the APFAL operation, consider Figs. 1 and 2. During the Evaluate phase T1, assuming HIGH IN and LOW / IN, At this time, with high OUT at its gate, the transistor MN1 conducts pulling the /OUT node low. This, in turn, augments the charging of OUT node by pushing MP2 also ON. Thus, during this phase, the charging path resistance is found to be that offered by the MP2-MN4 transmission gate structure. Hence, the harging path resistance for node OUT is

$$R_{on,char} = \left[\mu_{eff,p} C_{ox} \left(W_{eff,p}/L_{eff,p}\right)\left(V_{dd}/2 - 2|V_{th}|\right)\right]^{-1} \quad 1$$

Here, Vdd is the peak power-clock voltage, μeff,p is the mobility of the pMOS transistor in the charging path, Vdd/2 is the average gate to source voltage, Cox is gate oxide capacitance and W and L are the channel width and length of the transistors. Note that MP1 is OFF and MN1 is ON due to the high OUT at their gate

terminal. In the same way, MN2 is OFF with the logic LOW of node /OUT applied at its gate. During Hold phase T2, IN starts falling and MN4 continues conduction only until PC voltage is more than Vth, beyond which it stops conduction. During the Recovery phase T3, IN

is low and PC starts falling. This enables the charge recovery through the conducting device MP2. At this time, the recovery path is offered by the conducting MP2 with resist-

$$R_{on,rec} = \left[\mu_{eff,p} C_{ox} \left(W_{eff,p}/L_{eff,p}\right)\left(V_{dd}/2 - |V_{th}|\right)\right]^{-1} \quad 2$$

Thus, it can be noted that the recovery path resistance is more than that of the charging path resistance. Note that (1) and (2) express the Ron that approximates the midpoint of the PC slope during the charging/recovery phases. The Ron of the two output nodes happen to be the same for PFAL. On the other hand, the resultant *Ron* of the two output nodes of APFAL differ.

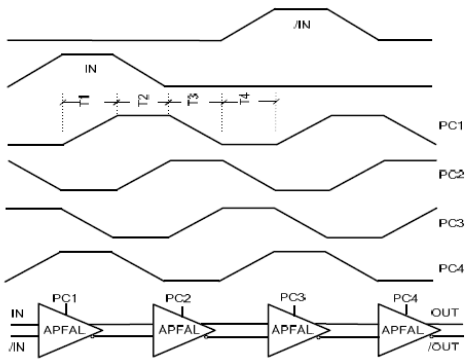


Fig. 2 Timing waveforms and inverter cascade

The resistance from PC to OUT node in APFAL during the Evaluation phase is

$$R_{on} = \left[\mu_{eff,p} C_{ox} \left(W_{eff,p} / L_{eff,p}\right)\left(V_{dd}/2 - 2\left|V_{th}\right|\right)\right]^{-1}$$

Then, the conduction happens through MP2 and MN4. However, when /IN is high, and when MP1 conducts, the corresponding value while charging the node /OUT is

$$R_{on} = \left[\mu_{eff,p} C_{ox} \left(W_{eff,p} / L_{eff,p}\right)\left(V_{dd}/2 - \left|V_{th}\right|\right)\right]^{-1}.$$

When /IN is HIGH, MN3 conducts providing perfect ground to OUT node. This avoids the floating output problem at the node OUT. This advantage is further discussed in the next ection. Figs. 3 and 4 show the signal transients of the PFAL and APFAL inverters respectively. The results are obtained in the same simulation environment at 200MHz frequency. From the transients, and the charging/recovery currents the following points are observed: (1) while the PFAL consumes 127fJ of energy for 40ns uration from the start of simulation, APFAL consumes only 68fJ. (2) The charging current values are 42uA for PFAL buffer and 36uA for APFAL buffer. (3) The transient impulses found in PFAL are steeper, with a magnitude of 5uA or 15% more than that of the APFAL, during both the charging and recovery processes. (4) The energy incurred by PFAL for two power clock durations is more than 35fJ. On the other hand, the corresponding value for APFAL is only 20fJ. This increased energy of PFAL is due to the larger C_L at /OUT also.

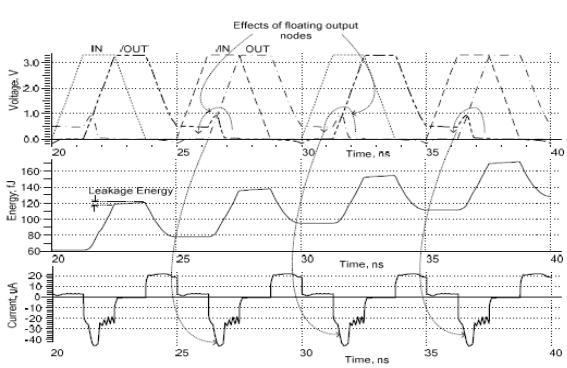


Fig. 3. Energy transients of the PFAL buffer

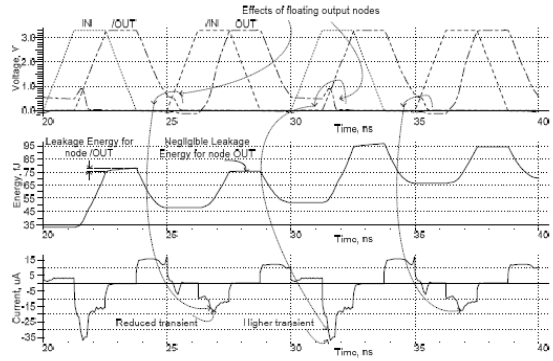


Fig. 4 Energy transients of the APFAL inverter

The *CL* at node /OUT of the PFAL is contributed by the drain-bulk junction capacitance Cdb of MN1, MN4 and MP1, the gate-drain capacitance Cgd of MP2 and MN3, gate-bulk capacitance Cgb of MN3, the gate-drain overlap capacitance Cgdo of MN4, the wire capacitance and the fan-out due to next stage. This load capacitance is the same at both the OUT and

/OUT nodes. On the other hand, *CL* of APFAL at node / OUT is very less, contributed only by the Cdb of MP1 and MN1, Cgd of MP2 and MN2, and Cgdo of MN2. This justifies the lower rise

in energy during the period from 25 ns to 30 ns for the APFAL in Fig. 3. Hence, the placement of the functional block in parallel with MN2 appreciably reduces the non-adiabatic energy spent during the charging process of the output node. Additionally, the comparison of the energy loss due to leakage, during the Hold phase for PFAL and APFAL in Fig. 3 indicates the following: (1) The Hold phase energy dissipation

of PFAL rises for each pulse. (2) However, the corresponding energy rise for APFAL is less. This is due to the negligible amount of energy raise that occurs, when the node / OUT with reduced *CL* is driven and due to the non-floating output node as shown in Fig. 4.

The APFAL and PFAL circuits were tested for toggling and non-toggling inputs. During toggling, the input alternately toggles between logic 1 and 0. This procedure brings out the effect of energy dissipation due to latch operation, the adiabatic energy dissipation and the (1/2)CV2 energy dissipation at the output nodes. During non-toggling input, the energy dissipation would be only due to the adiabatic component. The simulation for the toggling input conditions show 68 fJ for APFAL and 128 fJ for PFAL. The corresponding energy values for non-toggling input to APFAL depict 17 fJ for the

/OUT node and 82 fJ for OUT node, as against 78fJ for the PFAL buffer. Figs. 5 (a) and (b) show the energy transients for toggling inputs across 50 MHz to 500 MHz frequency range. The amplitude of the PC voltage varies from 2.5V to 3.3V. Consolidating, the total energy dissipation per cycle in the adiabatic circuit during a charge-recovery operation including the leakage and energy losses due to the latch

$$E_{diss} = \frac{2R_{on}C_L}{T} C_L V_{dd}^2 + \frac{1}{2} C_L V_{th,p}^2 + V_{dd} I_{Leak} kT + E_{opn} \quad 3$$

The second term indicates the adiabatic power dissipation due to the floating output node and it decreases greatly for APFAL.

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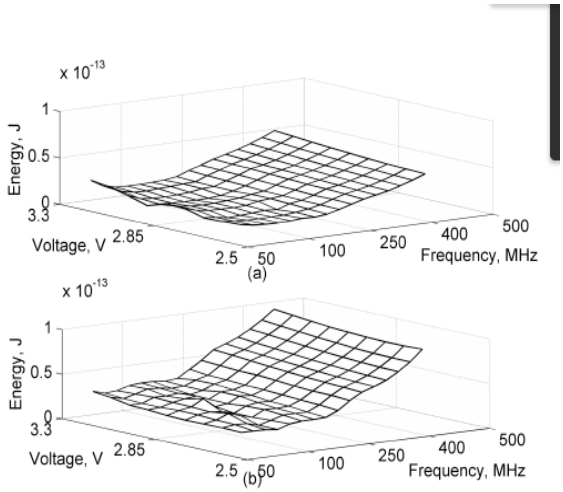


Fig. 5. Energy dissipation of (a) APFAL and (b) PFAL inverters

The third term attributes to the dissipation due to leakage. This leakage component is the current that passes through all the OFF transistors, in the path to, either the power-clock or the ground terminal. Note that the leakage current flows fork number of phases of power-clock, with k<4 for the four-phase

power-clock supply. The last term Eopn accounts for the power dissipation incurred in the latch operation [9].

III. ENERGY LOSS MODELS OF APFAL INVERTER

This section presents the loss models of APFAL, validated through pre-layout and post-layout simulations. To elucidate the models, consider the basic APFAL buffer/inverter of Fig. 1. It can be observed from (3) that CL accounts for the first, second and fourth energy dissipation components. Consequently, the reduction of CL in APFAL is managed in two ways. At the node /OUT, the load capacitance is that

offered by combination of MP1 and MN1 only. On the other hand, at node OUT, the asymmetric arrangement of functional blocks seemingly increase the CL=Cout value. However, the size of the F1 and /F1 ultimately decide the load capacitance. In the APFAL design, these devices are chosen to be of the minimum size. The size of MP2 mainly decides the charging/discharging path resistance Ron. Furthermore, the adiabatic pipeline operates with the complementary output signals obtained from

the previous stage. Since the two pull-up paths of the senseamplifier structure additively helps in the charging/recovery processes, the asymmetric structure imposed in the adiabatic pipeline helps in effective load capacitance reduction. It can be seen from Fig. 5(b) that the PFAL containing the functional blocks in the pull-up path dissipates more power than the APFAL counterpart of Fig. 5(a). More importantly, the reduction in CL also reduces the second component of power in (1). Thirdly, an appreciable reduction is achieved by the placement of /F in the path to ground, rather than the PC to /OUT path. Note that the position of the functional block F and /F in the path from PC to output nodes always incur leakage paths in the PFAL design. Moreover, this leakage component of power dissipation increases for complex functions such as NOR. This is due to the increased number of parallel leakage paths in PFAL.

The maximum frequency of operation realized by an adiabatic circuit depends upon the efficiency of the Evaluation and Recovery phases. That is, the Req C_L factor imposes restriction on the maximum frequency. Here, Req denotes the resistance offered by the effective Evaluate/Recovery paths. It can be noted that the functional block /F placed in the pulldown path is rather advantageous. This is due to the fact that the resistance offered by /F and the stacked transistors in /F reduce the leakage current, when the node OUT is at HIGH level. It can be argued that (1) the load capacitances at the two output nodes of the 2N-2P structure are dissimilar and (2) this could hamper the balanced load characteristics of adiabatic resonant power supplies. However, it is pointed out that the

logic functional blocks of PFAL by themselves are complementary. For instance, the NAND or NOR structures pose varying capacitance values at the output nodes. Additionally, the layout design of APFAL generates reduced parasitic capacitance due to the presence of one of the two complementary functional blocks in the pull-down arm itself. This results in easier layout with shorter interconnects, as against its parallel connection with the PMOS device of the PFAL latch.

IV. DESIGN PROCEDURE

The 350nm C35B4M3 CMOS technology from Austria Micro Systems is used for the pre-layout and post-layout simulations. Pre-layout simulation is carried out by extracting

the netlist from the circuit schematics, using Synopsys EDA tool. The post-layout simulation was done using the netlist extracted from the layout design. Hence, this includes the circuit parasitics also. The netlists from layout and schematic are compared using the layout-versus-schematic (LVS) tool. The AND, NAND, NOR, AND-OR, AND-OR-AND and XOR gates, and buffers for use in CLA circuits and multiplier circuits are some of the cells designed for the custom-designed library. Modular design flow was adopted in the designs, by the use of these cells. The modular level interconnections were done using the first three metal layers 1, 2 and 3 for multiplier circuits, and curtailing to only two metal layers for the CLA circuits. The circuit structures used for the validation of the design are 4, 8 and 16 bit Bent-and-Kung Carry-Look ahead Adders [8] and 4 and 8 bit multipliers [12]. The layout provides a continuous n-well across the cells for a row of gates. It facilitates horizontal power-clock wires at the top, which allows the input and output lines connect to the cells vertically from top and bottom. Fig. 6 shows the layout of a 16-bit CLA circuit. The input lines enter from the bottom and the outputs are available at the top. The power clock and ground

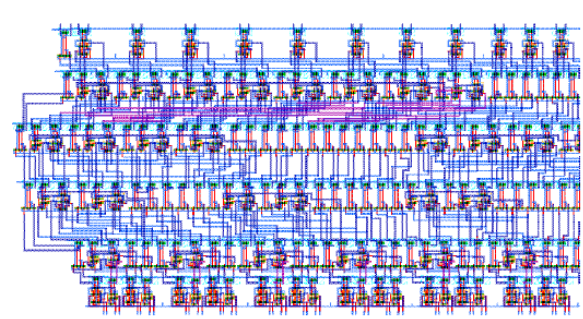


Fig. 6. A portion of 16-bit CLA adder layout

V. RESULTS AND DISCUSSIONS

This section compares the performance of APFAL circuits with CMOS and PFAL counterparts. Figs. 7 (a) and (b) show the APFAL power dissipation, adiabatic gain of APFAL and PFAL buffer/inverters taken for comparison

against the static CMOS inverter. Here, the adiabatic gain [8] is defined as the ratio between the power dissipation incurred by the static CMOS buffer and the APFAL buffer circuit. The comparison is made for the frequency range of operation from 50 MHz to 500 MHz. It can be observed that the adiabatic gain of PFAL varies from around 9.5 to 4 across 50 MHz to 500 MHz frequency range. The corresponding gain values of APFAL are 17.5 and 6.3 for the same frequency values. Changing the width of the harging/discharging path of the APFAL and

optimizing the size of the transistors in the complementary functional blocks lead to efficient power and frequency performance characteristics. Thus, the drivability or the

required fan-out and adiabatic gain can be achieved. Though the results shown are for Typical or the Mean model of AMS process, the Worst case Power and Worst case Speed

models as well were verified for validating for proper functioning of the circuits. The comparisons with static CMOS circuits were made using our custom designed cells of the same technology for justifiable performance comparison. Table I shows the layout area comparison of APFAL and PFAL circuits. The number of transistors remains the same for both the circuits. However, the layout area differs with the APFAL achieving reduced layout complexity than the PFAL circuits due to the change in placement of the functional blocks.

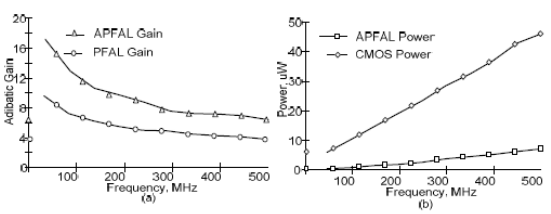


Fig. 7(a). Adiabatic gain of APFAL buffer vs. PFAL and (b). Power dissipation of APFAL and CMOS buffers

TABLE I COMPARISON OF APFAL AND PFAL CIRCUITS

Arithmetic circuit	Layout Area, um² (PFAL)	Device(#) APFAL & PFAL	Layout Area of APFAL in um² (PFAL /APFAL)
4-b CLA	6441	278	4771 (1.35)
8-b CLA	16478	700	13078 (1.26)
16-b CLA	40861	1706	34051(1.2)
8-b multiplier	295099	8660	247982 (1.19)

TABLE II ADIABATIC GAIN OF APFAL AGAINST CMOS CIRCUITS

Arithmetic Circuit	Frequency, MHz		
	100	*200*	*500*
4-b CLA	19.14	18.13	10.76
8-b CLA	15.32	13.87	8.56
16-b CLA	12.87	9.76	7.12
8-b Multiplier	14.91	13.5	6.45

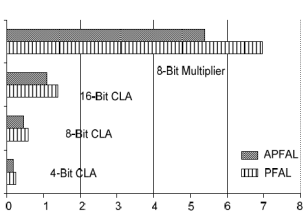


Fig. 8. Energy comparison between APFAL and PFAL circuits

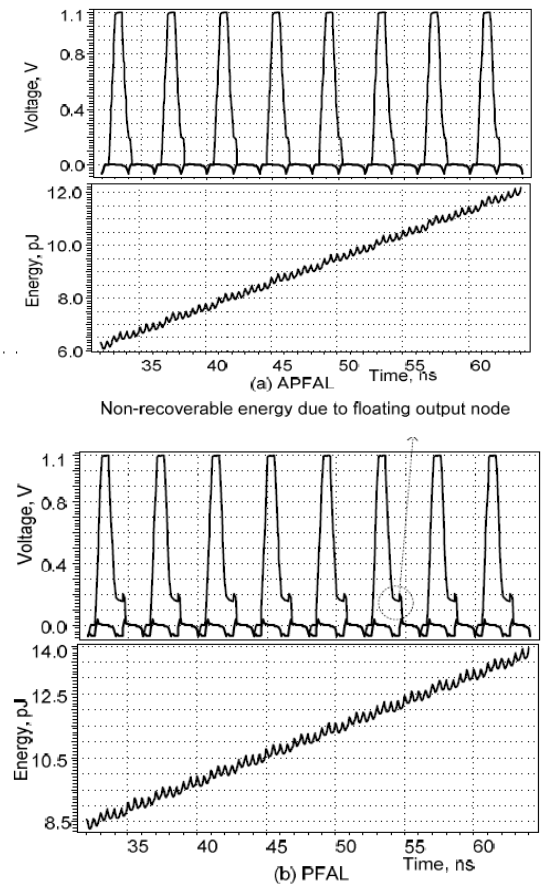


Fig. 9. Output and energy transients of 8-bit multiplier circuits (a) APFAL and (b) PFAL

The energy dissipation comparison between PFAL and APFAL are shown in Fig. 8 obtained through post-layout simulation studies. The results of Figs. 3 and 4, and Tables I and II are obtained using 350 nm AMS technology library. However, the simulations were also run for the 130 nm, 90 nm and 65 nm technology models obtained from Berkeley

Predictive Technology Model BPTM [13]. This proved the feasibility of APFAL design for lower technology nodes also. Figs. 9 (a) and (b) show the output and energy transient

waveforms of APFAL and PFAL 8-bit multiplier circuits obtained using High Speed 65 nm BPTM technology models, operating at 1.1 V power-clock voltage. The energy dissipation of APFAL is 12 pJ against the 14 pJ of PFAL. The output transients of PFAL can also be observed for their floating output nodes, with their magnitude reaching 0.3 V. The threshold voltage of the 65 nm technology used is 0.19 V for High Speed and 0.39 V for Low Leakage models.

VI. CONCLUSION

The Asymmetric Positive Feedback Adiabatic Logic is proved capable of perating up to 500 MHz with reduced power. It needs less complex layout design and smaller layout area. The APFAL design results in glitch-free circuit also with reduced floating node problem prevalent in PFAL counterpart. The effect of optimally placed NMOS functional blocks in the pull-down arm eliminates the floating node problem of the 2N2P latch of PFAL logic. This structure additionally realizes reduction in the output nodal capacitance and minimum leakage paths. The operating capability of APFAL is validated using post-layout simulation of

Volume : 5 | Issue : 10 | October 2016 • ISSN No 2277 - 8179 | IF : 3.508 | IC Value : 69.48

4-b, 8-b and 16-bit CLAs and multiplier designs. Comparison is made with conventional CMOS circuit counterparts and PFAL circuits.

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