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An Experiment on Reading Disability of the Children with Specific Learning Disability – An Intervention Study

Mahendran. S Final ME-PED, Paavai College Of Engineering, Anna University-Chennai

Mr. D. Saravanan Professor & Head / EEE, Paavai College Of Engineering

ABSTRACT

This modulation method is based on selective virtual loop mapping, to achieve dynamic capacitor voltage balance without the help of an extra compensation signal. The concept of virtual submodule (VSM) is first established, and by changing the loop mapping relationships between the VSMs and the real submodules, the voltages of the upper/ lower arm's capacitors can be well balanced. This method does not requiring sorting voltages from highest to lowest, and just identifies the MIN and MAX capacitor voltage's index which makes it suitable for a modular multilevel converter with a large number of submodules in one arm. Compared to carrier phase-shifted PWM (CPSPWM), this method is more easily to be realized in field-programmable gate array and is conducive to the control of circulating current. Its feasibility and validity have been verified by simulations.

KEYWORDS : Dynamic voltage balance(DVB), modular multilevel converter (MMC), phase disposition pulse width modulation (PDPWM), Photovoltaic (PV), selective virtual loop mapping (SVLM)

I. INTRODUCTION

In recent years, with the development of a large-scale photovoltaic (PV) power plant system, as well as smart grid and multilevel technologies, higher requirements in voltage level, modular structure, and flexibility and reliability of the next-generation large-scale PV grid-connected inverter have been put forward. The features include the following:

1) Power peaking capacity: PV systems should be able to store the electrical energy which is issued by itself as needed during light load conditions; meanwhile, this part of electrical energy would be released again for the load when the load is at the peak. As a result, the peak power of the grid and the reliability of power supply can be improved.

2) Fault ride-through capacity: A large-scale PV system has been required to have the ability to withstand short periods of voltage abnormality, such as the voltage short-term drop caused by short-circuit fault. The PV system should maintain the connection of the inverter and the grid in addition to providing support to the grid.

3) Power quality control: More stable power supply performance could be achieved by introducing suitable inverter control strategy including voltage stability, phase regulation, active filter.

4) Higher redundancy and error correction capacity: The PV system should have the capacity to work efficiently when the failure occurs in some of the modules of the inverter system and should be "smart" enough to correct the situation.

The aforementioned requirements drive the research and development of the next-generation PV inverter, and the topologies of utility PV inverters are moving toward multilevel structure,which could provide better harmonic spectra and reduce the weight of the filtering components.

In many of the multilevel structures, a modular multilevel converter (MMC) has attracted many researchers recently. MMC-related application research has mostly concentrated on high-voltage direct current transmission, high-power motor drives, integrated energy storage and medium-voltage STATCOM.The MMC used in the PV grid-connected system is just mentioned in the reasons of this situation are as follows:

II. PROPOSED METHOD

a) Phase Disposition PWM

To overcome the previous disadvantages we proposed a new selective virtual loop mapping (SVLM) method based on phase

disposition PWM (PDPWM) which has voltage balance capability. The concept of virtual submodule(VSM) is established, and by changing the mapping routines between the VSM and the real submodule(RSM) with SVLM, the capacitor voltages of the upper and lower arms can be balanced even if the inverter loses its symmetry. The method has been designed to consider the following situations: 1) no extra signal should be added to the reference voltage to provide a good basis for the suppression of the circulating current; 2) the possibility of a large number of submodules in one arm; 3) retain the equivalent switching frequency of the PDPWM; 4) it could be easily realized in field-programmable gate array (FPGA) for a large-scale converter which has a large number of submodules.As an important modulation method, carrier disposition (CD) PWM has been widely used in multilevel modulation, and it can be divided into three types: phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD). For simplicity, this paper will focus on the PDPWM to discuss MMC modulation. PDPWM has been studied for MMC modulation in orderto balance capacitor voltages, rotating carrier waves were used, but it seems that they can only work under symmetric condition.

1) First, all of the individual capacitor voltages are compared, and the corresponding RSM indexes of the maximum voltage and minimum voltage are obtained. The MIN index block diagram is shown in Fig. 6(a) (N =4). Y is an array, and Y (1) is the first element. Udc1 − Udc4 are the SM's capacitor voltage of the upper arm separately and they are compared to each other at the same time which means that the time is limited. Y (1) would be equal to the capacitor index havingthe minimum voltage: for example, if the voltage of Udc3 is the minimum, Y (1) would be equal to 3. Priority check is just for the case of more than one input of X1–X4 equal to 1, so that X1 could be set up to the highest priority in the MIN check, while X4 has the lowest priority. For the MAX check, "≤" would be replaced by "≥," while Y (2) provides the corresponding index of the maximum capacitor voltage [see Fig. 6(b)], and X4 should have the highest priority while X1 should have the lowest priority.

V. OPERATING PRINCIPLE OF PHASE DISPOSITION PWM METHOD

a). Modulation Principles

Fig. 10 shows the single-phase equivalent circuit of the MMC, which has two arms including the upper arm and the lower arm, with each arm having N submodules (SM), one buffer inductor L, and equivalent resistor R. The dc link of the MMC is floated or connected to high-voltage sources depending on the working purpose of the converter. The output of the converter is the connection point of the upper and lower arms. Ls is the ac-link inductor, and $Z0$ is the equivalent impedance of the ac side. The working states of SM are shown in TableV. Each SM has two states ("ON" and "OFF"), and the corresponding output voltage (Usm) of the SM is Vc or 0.

VII.EXPECTED RESULTS

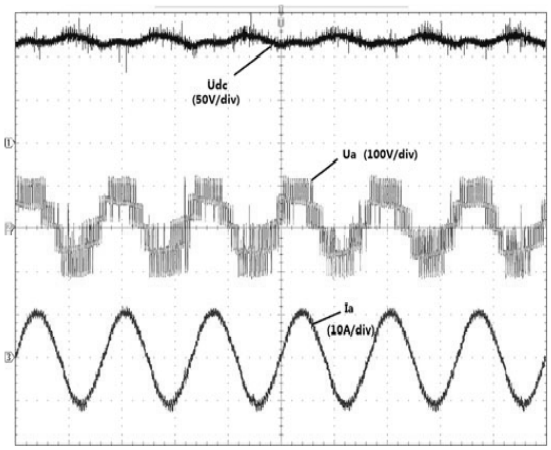

Fig. 12. DC-link voltage, output voltage, and output current

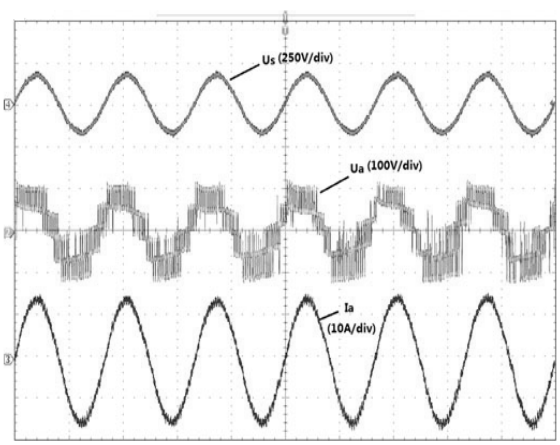

Fig. 13. Grid voltage, output voltage, and output current inverter.

VI.CHALLENGES IN PROPOSED CONVERTER

The capacitor voltages of the upper and lower arms can be balanced even if the inverter loses its symmetry. The method has been designed to consider the following situations: 1) no extra signal should be added to the reference voltage to provide a good basis for the suppression of the circulating current; 2) the possibility of a large number of submodules in one arm; 3) retain the equivalent switching frequency of the PDPWM; 4) it could be easily realized in field-programmable gate array (FPGA) for a large-scale converter which has a large number of submodules.

VII.CONCLUSION

This paper first discussed the possibilities of the MMC being used as an interface between the grid and PV panels, and proposed an improved SVLM method based on the PD PWM .This method can produce $2N + 1$ and $N + 1$ level outputs in the MMC, and achieve submodule capacitor voltage dynamic balance compensation control while not changing the reference signal. The whole mapping rules are presented and it is easy to be implemented in FPGA and the effectiveness of the method was proved well.

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