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Research Paper Engineering

Design And Implementation Of Ethernet Controller On Fpga

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ABSTRACT

Today is demand of data communication with very high level. It is possible to acquire data from any field at our home or office. It is possible to combine control with our desired data which require for completing our specification. After programming it will become ASIC (Application Specific Integration Circuit).For communication at network layer, The Ethernet full-duplex protocol is easy to implement in an FPGA. FPGAs are very powerful, relatively low-cost, and adjustable, since their configuration is specified in an abstract hardware description language. There are many tools available In FPGA which gives idea about Input/output, The Chip Scope Pro Serial I/O Toolkit provides features and capabilities specific to the exploration and debug of designs that use the high-speed serial transceiver I/O capability of Xilinx FPGAs. RJ-45 is used for communication over Ethernet.

KEYWORDS:Ethernet,DataCommunication,IPV4,FPGA-SPARTAN3E,ChipScope,Wireshark

INTRODUCTION

The development of FGPA-technology has advanced in terms of usable resources, number of gates, processing speed, energy consumption & retail prices [1, 2].Recently the FPGA based system has many compensations of DSPs & ASICS because of their high description language, reusability, moderate cost, feature expansion[4]An FPGA consists of an array of programmable logic blocks interconnected by programmable routing resources. The Programmability and configurability of FPGA allow it to be used for a variety of digital applications from small finite state machines to large complex systems. As a substitute of application specific integrated circuit (ASIC), the fast time-to-market and low NRE cost drove it to develop at an astonishing speed[3].Data communication on Ethernet is very high speed networking, because it is the most valuable property for data sharing & exchange[5]. Embedded system is made for performing the specific task which desired by user. For that various processors are used, but here for getting some specific advantages FPGA used, because here the user can design chip with using of HDL (Hardware Description Language).The mixture of FPGA & Ethernet gives the design of chip, by which we can apply that particular chip in specific application. So I have decided to make the Ethernet chip and use that chip for any embedded application. For that I have used temperature control system using RTD for temperature sensing and receive data to .One can see data at PC from any field with Ethernet

Section II shows the summary of SPARTAN3E, Ethernet, Ethernet frame, data communicationIPV4.Section III shows the work for communication with FPGA done by different researchers in brief. Section IV shows the Implementation method for receiving frame in FPGA. Section V shows the Simulation result. Section VI shows Conclusion. Section VII shows the references.

II.SUMMARY

SPARTAN-3E

The Spartan®-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates. Figure 1shows the image of SPARTAN 3E [8].



Figure 1. SPARTAN3E

.ETHERNET

A local-area network (LAN) protocol developed by Xerox Corporation in cooperation with DEC and Intel in 1976[13]. Ethernet uses a bus or star topology and supports data transfer rates of 10/100/1000 Mbps [13].The Ethernet specification served as the basis for the IEEE 802.3 standard, which specifies the physical and lower software layers Ethernet uses the CSMA/CD access method to handle simultaneous demands. Figure2 shows the Ethernet Frame format [9].

Preamble (7 Bytes)	Sfd (1 Byte)	Destination Address(6 Bytes)	Source Address (6 Bytes)	Type/Length (2 Bytes)	Data (46 Bytes)	CRC (4 Bytes)

Figure2.Ethernet Frame Format

A node starts transmission by sending an 8 byte (64 bit) preamble sequence [9]. This consists of 62 alternating 1's and 0's followed by the pattern 11[9]. Strictly speaking the last byte which finished with the '11' is known as the "Start of Frame Delimiter"[9].After that there are destination & source address of machine for which data can be communicated [9].Then details of protocol by which data should be received, Cyclic Redundancy Check k for making free from errors[9]. Ethernet defines the lower two layers of the OSI Reference Model [13].

A.DATA COMMUNICATION:

Data Communication are the exchange of data between two device via some form of transmission medium such as wire cable. The effectiveness of a data communication system depend on four fundamental characteristics: delievery, accuracy, timelines, jitter [17]. Figure 3 Data communication system has five components shown in figure [17] & its functions are in Table I.

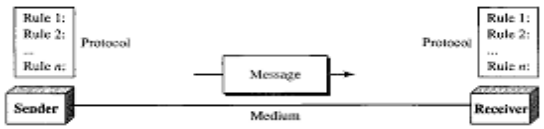


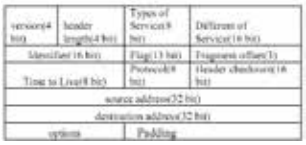
Fig 3.Data communication

B.IPV4

Figure 4 shows the ipv4 data gram for data communication and their explanation as shown in table I.

Table I.IPV4 explanation

Figure 4. IPV4 datagram



III. REVIEW OF RESEARCH

The physical layer (PHY) interface constitutes a link between the physical signals transmitted on the network and the digital environment on the FPGA. It communicates with the MAC layer via Media Independent Interface (MII) which is an industry standard interface for PHY devices. As long as the PHY device uses MII the communication between the PHY device and the MAC layer is the same, the only difference is the speed of the data transmission. This means that the system designer does not need to consider whether the physical network consists of a 10 Mbit or 100 Mbit twisted pair network or even a fiber optic network [6].

Each byte within a field is registered by a counter. When count value is reached; the state is changed [20].

The Ethernet controller can be classified into four main components namely [5].

1. System interface unit: Connecting the host system
2. Local memory unit: Where the data is buffered temporarily.
3. CSMA/CD unit: Core performing Ethernet controller function.
4. Serial interface unit: Connection to the network.

The traffic that goes on an Ethernet is transported in frames of data with a definite beginning and a definite end [5].In the 'preamble' and 'sfd' states, the preamble and the sfd fields are built and chained to the frame. After Ethernet address match of two machines data receiving process starts. CRC is calculated both at the transmitting & receiving end for error free communication [5].

IV. DESIGN METHODOLOGY & IMPLEMENTATION METHOD

The flow of receiving bit in Ethernet frame will be preceded according to figure as show below in figure5. In this first 7 byte(55555555555555) have been received, then 1 byte (d5)have been received, Then Machine address from which data have been received, It should be 6 byte, The data at which data have been received It should be 6 byte. Then the type of data by which the flow of data have been receive in network layer with IPV4,IPV6,ICMP.Here the receiving design is according to IPV4. For that identification, flag, protocol number by which transmission of data should be received with control. Then IP (internet Protocol) source address & destination address should be received. Then CRC (Cyclic Redundancy Check) has been received. This section shows the implementation of Ethernet frame into FPGA.It is possible to receive data through PIC, Microcontroller or PLC.But in FPGA there are some more features included like LVTTL (Low Voltage Transistor Transistor Logic), LVCMOS (Low Voltage CMOS), HSTL (High Speed Transceiver Logic), SSTL (Stub Series Terminated Logic).

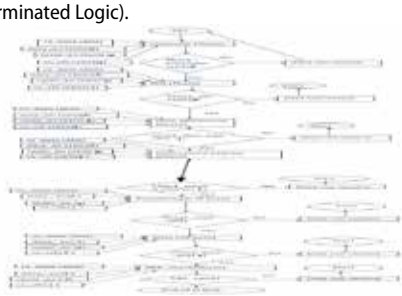


Figure 5.Design of Ethernet frame

A. SIMULATION RESULT

Figure 6, 7 shows the simulation results of preamble verification, sfd verification, source address & destination address verification, udp port verification ,data verification for data receiving accordingly.

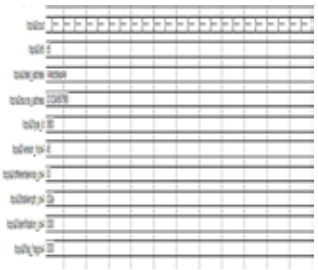


Figure 6.Data verification with Preamble Flag, Fragment, and Dest_address verification

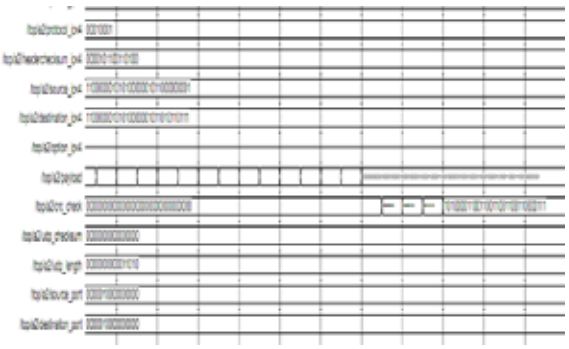


Figure 7.Udp port verification

VI .IMPLEMENTATION RESULT

The Spartan 3E kit load data by Xilinx USB cable so it is possible to see data in PC by Chip scope Analyzer. Use of ChipScopePro Virtual I/O for providing input to the BlockRAMaddress/data/write enables busses. Figure 8 shows the program will be run successfully. Figure 9 shows Ethernet data verification at spartan3E



Figure 8.Program execution



Figure 9.Data verification in Spartan 3E

VI.CHIPSCOPE ANALYZER

For debugging FPGA design using the Xilinx® Chip Scope™ Pro tool. The Chip Scope Pro tool comprises the Chip Scope Pro cores in the CORE Generator™ software, the Chip Scope Pro Core Inserter, and the Chip Scope Pro Analyzer. Figure 10 shows the Destination verification in spartan3E



Figure 10.Destination verification

VII.DATA RECEIVING FROM EMBEDDED SYSTEM

Wire shark is Open Source Software released under GNU General Public License. It is used for data receiving according to Protocol which define in Ethernet frame. We have to define ip address to spartan3E.One is PC.figure 11 shows the Ethernet wire with cable. Figure 12 shows the

data from spartan3E



Figure 11.Configuration for Ethernet

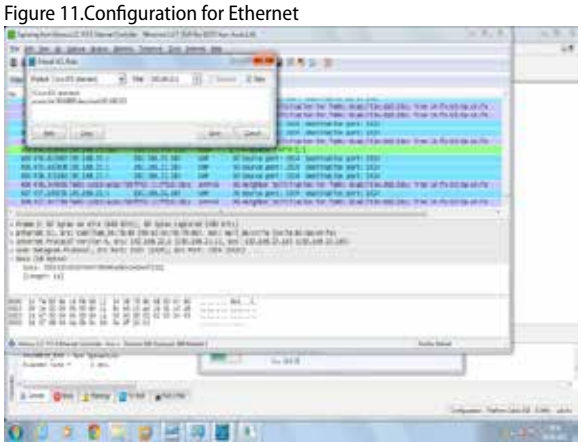


Figure 12 Real time data

A.EMBEDDED SYSTEM DESIGN

Figure 13 shows circuit diagram for receiving digital data at wire shark protocol analyzer. Here RTD is used to sense the temperature, according to that change in temperature, variation in voltage in terms of milivolt, That will be amplified by OP-07 operational amplifier, then it will go to ADC 0804, 8 bit data load into FPGA.FPGA SPARTAN-3E gives that data to PC using RJ-45.

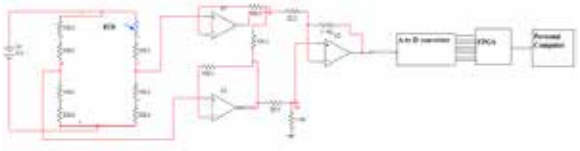


Figure 13.Circuit diagram

Figure 14 shows the image of ADC 0804 (Analog to Digital Converter) that will be go into SPARTAN-3E.



Figure 14.Image of Spartan -3E Connection to ADC

Figure 15 shows the Network Status after configuring the Internet Protocol address of SPARTAN-3E & PC



Figure 15 LAN status

Figure 16 shows data can be received in UDP receiver application which can shows the real time data update with change in temperature.



Figure 16.UDP receiver

Figure 17 shows the data have been received in wire shark with detail of address port with ip address 192.168.22.1 of SPARTAN 3E & ip address of PC is 192.168.22.8.

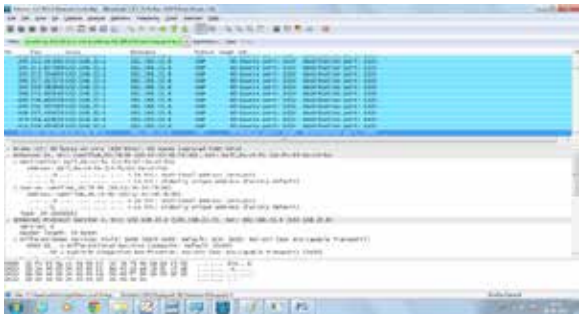


Figure 17 Data dispatch in Wire Shark

VIII.CONCLUSION

From this analysis for receiving data through Ethernet we require 20 MHz frequency, but SPARTAN3E kit has 50Mhz.So there is 20 MHz frequency. Real time data can be received using RJ45 cable tester. In this the components used to make this ASIC are:136 slices from 9312,135 flipflop,4 input LUT 158 from 9312.From this it can be proved that very less area used for data receiving. Design of Ethernet controller has been 70% completed by using state machine logic because modules have not been port mapped as they had problem individually [5]. Instead of state machine design, the condition of Ethernet protocols are used in this proposed design has zero error and all the Ethernet protocol modules like Preamble, SFD, Mac destination address, Mac source address, types, data, and checksum verification are working properly & sequentially in Chip Scope Analyzer (version 10.1).The Verilog code for Ethernet protocol is implemented on Spartan -3E kit successfully.Spartan-3E kit received data which comes from Analog to Digital Converter which are in digital form. The input to Analog to Digital Converter is output of RTD, PT-100,2 wires. The PC receives the data transmitted using differential Manchester coding by Spartan-3E kit using RJ-45 Ethernet cable.

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