Volume-4, Issue-5, May Special Issue-2015 • ISSN No 2277 - 8160

Research Paper Engineering

DESIGN OF ADD-MULTIPLY OPERATOR USING AN OPTIMISED AND MODIFIED BOOTH RECORDER

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ABSTRACT

The Applications of Digital Signal Processing (DSP) are mainly based on the arithmetic operations. The proposed method is purely dependant on modified recoding techniques for booth recoding in DSP application. In MB (modified booth) form the summation of two numbers are done by the direct recoding, known as 'fusion technique'. This proposal is to implement the direct recoding of the multiplier in its Sum Modified Booth (S-MB) form. The proposed S-MB is simple, structured and can be easily modified for odd or even numbers. It is optimized with three different recoding schemes S-MB1, S-MB2, and S-MB3. By incorporating these techniques in fused Add-Multiply designs, which yields considerable reductions of critical path latency, complexity of hardware implementation and utilization of power of the Fused Add-Multiplier (FAM) design.

KEYWORDS : Modified Booth recoding, Add–Multiply Operation, Critical path delay, VLSI Design, Fused Add - Multiplier.

I.INTRODUCTION

Digital Signal Processing (DSP) is extensively used in the consumer electronics these days. In DSP applications, a large number of arithmetic operations are implemented by intensive kernels, such as Discrete Cosine Transform (DCT), Fast Fourier Transforms (FFT). The performance of the DSP application can be exaggerated by a large number of arithmetic operations which requires huge architecture. In latest researches the design optimization of arithmetic components which combining operations, can lead to significant performance improvements. In DSP algorithms the MAC and MAD [1] operators are the most efficient implementations. Several designs are proposed to optimize the performance parameters like area, critical path latency [2],[3],[4] related to Add-Multiply operations [5]. In the design of AM operator the Adder and multiplier are allocated as different blocks where the inputs are first given to the adder then the output is driven to the multiplier as an input. The straightforward design of AM operator, the area and critical path delay are significantly increased.

We optimize the design of AM by combining the adder and the MB encoder in the multiplier then the delay and the area are reduced. In MB form the sum of the two numbers is done by the direct recoding this technique is known as fusion technique [6], [7]. By this optimization which yields considerable reductions in critical path delay, area complexity and the power consumption. This fusion technique [8], [9] at Modified Booth recoder technique leads to a more effective implementation of the Fused Add Multiply (FAM) unit compared to the previous recoding schemes.

This methodology mainly based on the design optimization of FAM operator. The fused add multiply design consumes less power than the other existing designs. The proposed Sum-Modified Booth recoding [8],[9],[10] techniques are utilized to present the direct recoding [11] of the summation of two numbers in its MB form. The proposed sum-modified booth recode is explored into three different techniques by utilizing them in FAM design leading to considerable reductions in critical path latency, power utilizations and area occupation.

II. MOTIVATION

In the conventional design of AM operator implements the operation X=Y.(A+B). Where the input A and B are first driven to adder then the resultant output Z is send to the multiplier as an input and then Z and Y are driven to the multiplier in order to get X. The main drawback of using an adder in AM design the significant delay will occur in the critical path. In order to decrease this delay Carry Look Ahead adder can be incorporated, however the area complexity and power consumptions increase. To avoid these limitations an optimized design is invented, which is known as fusion technique in this the adder and the MB encoding in multiplier are combining into a single block by direct recoding then the delay can be reduced.

The proposed fused add-multiplier the sum Z=A+B can be done by the direct recoding, which contains only one adder parallel to the multiplier.

A) Modified Booth Form

The Modified-Booth (MB) algorithm is widely used for multiplier circuits [12],[13],[14] having enhanced speed. Use of array multipliers leads to the reduced number of partial products hence improving multiplier performance.

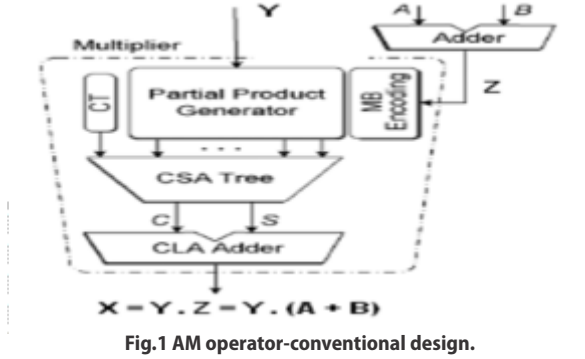


Fig.1 AM operator-conventional design.

By taking the 2's compliment numbers Y and Z multiplication with each number consisting of n=2k bits. The multiplicand Z can be represented in MB form [13],[15].

$$Z = -z_{2k-1}.2^{2k-1} + \sum_{i=0}^{2k-2} z_i.2^i$$

$$Z = \sum_{j=0}^{k-1} z_j^{MB}.2^{2j} \qquad (1)$$

$$z_j^{MB} = -2z_{2j+1} + z_{2j} + z_{2j-1} \qquad (2)$$

Digits $z_j^{MB} \in \{-2, -1, 0, +1, +2\}$, $0 \le j \le k-1$, correspond to the three consecutive bits $z_(2j+1)$, z_2j,$z_(2j-1)$with one bit overlapping and consideringthat $z__1=0$.

B) Fused Add-Multiplier Implementation

In FAM design in fig.2, based on the MB algorithm, the multiplier used is a 'parallel-one' based. Consider the product Y. Z. The term Z=<y_{n-1} y_{n-1},.....y_1 y_0 >$_{2's}$. Both Y and Z consist of n=2k bits and are in 2's complement form. The following equation describes the generation of the k partial products

$$PP_j = Y.Z_j^{MB} = \bar{p}_{j,n}2^n + \sum_{i=0}^{n-1} p_{j,i}.2^i \qquad (3)$$

On generating the partial products (PP's), we use a Wallace Carry-Save Adder (CSA) tree with the Correction Term (CT) to add and weigh. This is described by the below equation.

$$X = Y.Z = CT + \sum_{j=0} PP_j 2^{2j} \qquad (4)$$

$$CT = CT(low) + CT(high)$$

$$= \sum_{j=0}^{k-1} c_{in,j} + 2^n\left(1 + \sum_{j=0}^{k-1} 2^{2j+1}\right) \qquad (5)$$

$$\text{Where } c_{in,j} = (one_j \vee \vee two_j) \wedge s_j$$

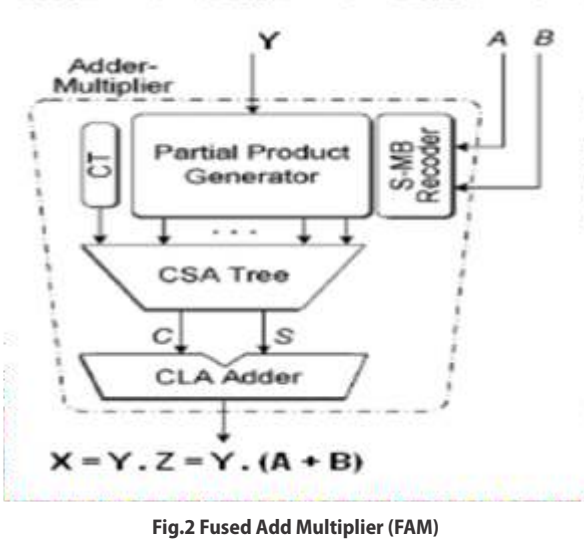


Fig.2 Fused Add Multiplier (FAM)

At last, the output from the Wallace CSA tree is given to the fast carry look ahead adder (CLA) and the final result is obtained as, X=Y.Z as shown in fig.2.

The AM operator [15] based on the conventional design is as shown in fig.1. The proposed design around which our work revolves is the fused design with direct recording of the addition of A and B. It is basically a parallel-based multiplier which is based on the modified booth algorithm. The adder and the MB encoding blocks in the existing system are combined to form a S-MB recorder block in the proposed system. The 'sum-modified booth' (S-MB) is the optimized block in the proposed system.

III. Proposed Method (Sum to Modified Booth Recoding Technique)

In our proposed technique we recode the summation of two bits of input A with two bits of input B into one MB digit. The MSB of it is weighted negatively on contrary to its LSB which is weighted positively. Here two different HAs (HA*, HA**) are used whose operation is described in below fig.3.

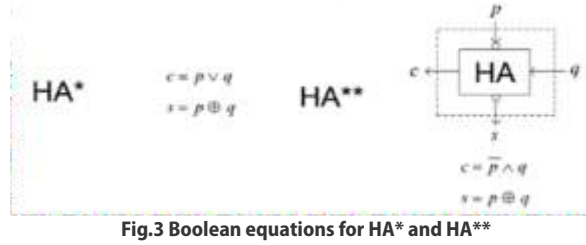


Fig.3 Boolean equations for HA* and HA**

In addition to this, we model two types of signed FAs (FA*, FA**). Their schematics and inter relation is shown in fig.4.

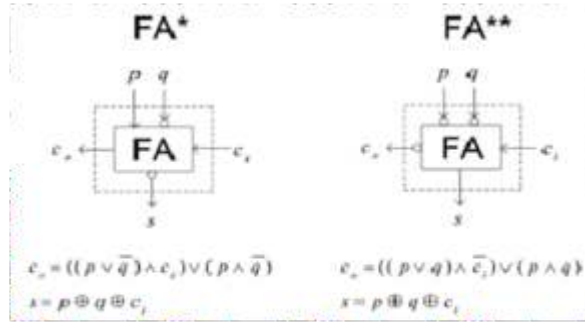


Fig.4 Boolean equations for FA* and FA**

All the above mentioned HAs and FAs are used in exploring three new schemes of the S-MB Technique. All these schemes can be easily implemented in signed and unsigned numbers with any numbers of bits. We shall discuss about each of them in detail.

A) S-MB1 Recoding Scheme

In this technique we adopt the same method in both the cases of even and odd number of bits except that we use an extra FA** in case odd number of bits. This process is illustrated in fig.5.

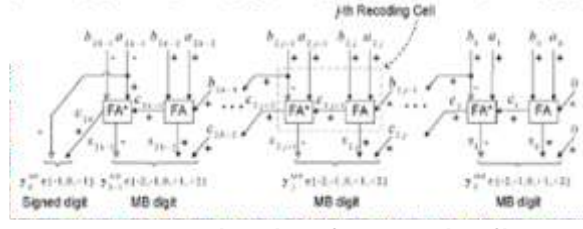


Fig.5 S-MB1 recoding scheme for even number of bits

From fig.5 the sum of A and B is give by the equation

$$Z = A+B = y_k.2^{2k} + \sum_{j=0}^{k-1} y_j^{MB}.2^{2j}$$

$$\text{Where } z_j^{MB} = -2s_{2j+1} + s_{2j} + c_{2j} \qquad (6)$$

The S_{2j+1} and S_{2j} are obtained from the j-recoding cell as shown in figure. The conventional FA whose inputs are a_{2j}, b_{2j} and b_{2j-1} gives the carry

$c_{2j+1} = (a_{2j} \wedge b_{2j}) \vee (b_{2j-1} \wedge (a_{2j} \vee b_{2j}))$ and the sum $s_{2j} = a_{2j}$ XOR b_{2j} XOR b_{2j-1}.

Now for the FA* the carry and sum are given as

$$C_{2j+2} = (a_{2j+1} \wedge \bar{b}_{2j+1}) \vee (c_{2j+1} \wedge (a_{2j+1} \vee \bar{b}_{2j+1}))$$

$$S_{2j+1} = a_{2j+1} \text{ XOR } b_{2j+1} \text{ XOR } c_{2j+1} \quad (7)$$

When the MSB of S-MB1 recoding scheme is obtained it can be distinguished into two cases of which the first case comprises of even bit of width A and B, while the second case comprises of both odd number of bits with respect to input bit width the S-MB1 has a constant critical path delay.

$$T_{S-MB1} = T_{FA,carry} + T_{FA*,sum} \quad (8)$$

B) S-MB2 recoding scheme

This method is similar to the former one but is differentiated with it over the use of half adders instead of full adders .this is shown in fig.6.

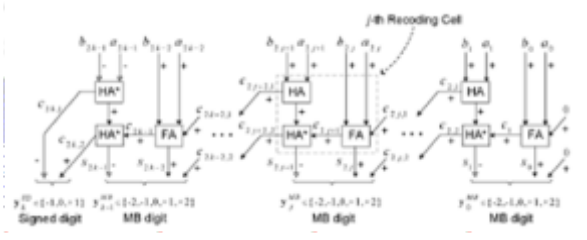


Fig.6 S-MB2 recoding scheme for even number of bits

This recoding scheme is almost the same for even and odd number of bits except that an extra FA** is used in the odd case. Overall the components used in the scheme are HA, HA*, FA, FA**.
The critical path delay mentioned below.

$$T_{S-MB2} = T_{HA,carry} + T_{FA,carry} + T_{HA*,sum}$$

C) S-MB3 recoding scheme

This third scheme is as shown in fig.7 below.

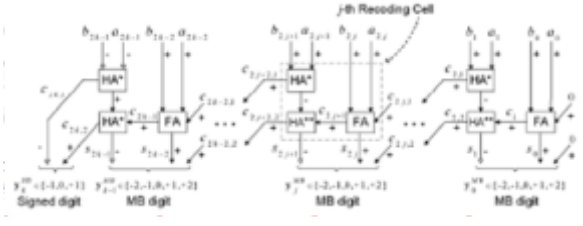


Fig.7 S-MB3 recoding scheme for even number of bits

The process is identical to the previous ones with an extra FA** added in the odd case .Here HA* and HA** along with FA and FA** are used .The critical path delay is calculated as

$$T_{S-MB3} = T_{HA*,carry} + T_{FA,carry} + T_{HA**,sum}$$

D) Unsigned Input Numbers

Here the input numbers A and B are taken which are unsigned .previous methods reveal the modifications that we need to make in all S-MB schemes in both even and odd cases regarding the signs of MSB s of A and B .but the basic recoding block is the same in all cases.

Even in this case there are three different schemes which are almost identical except that an unsigned bit is added in every odd case.

IV. Experiment and Results

The three proposed schemes are introduced in FAM design the resultant outputs are shown below.

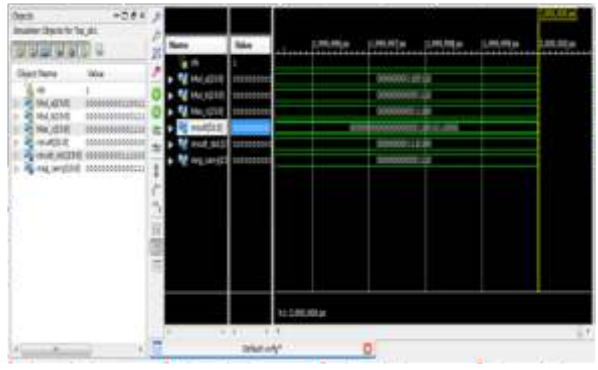


Fig.8 Output of S-MB1 scheme

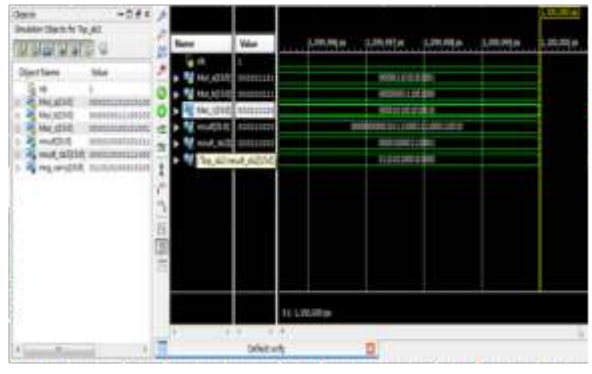


Fig.9 Output of S-MB2 scheme

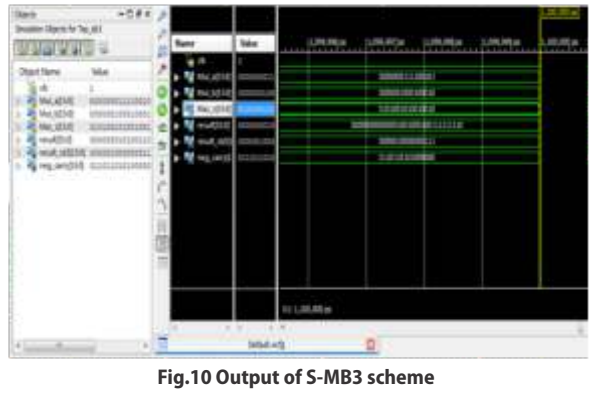


Fig.10 Output of S-MB3 scheme

The RTL Schematic showing the critical paths of S-MB1 and S-MB2 techniques are shown below. In a similar manner we obtain the RTL schematic for the S-MB3.

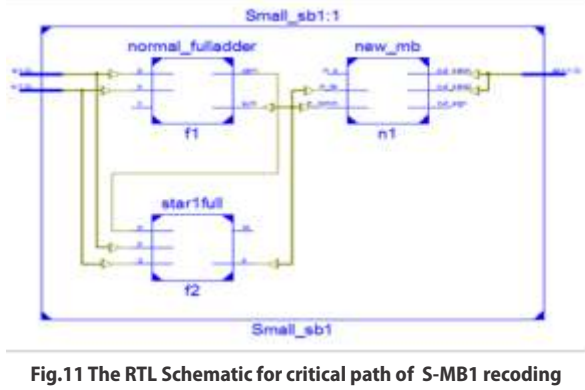


Fig.11 The RTL Schematic for critical path of S-MB1 recoding scheme

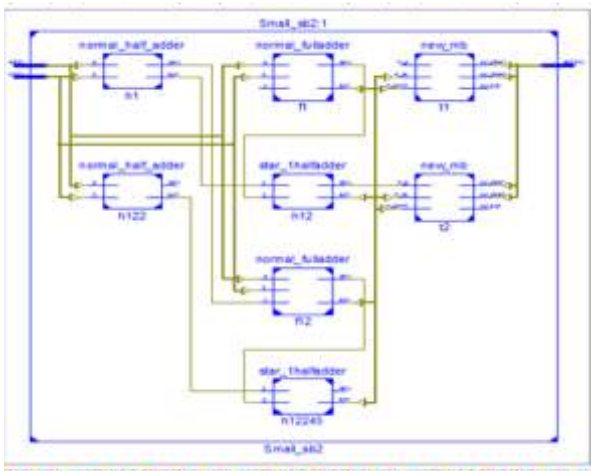


Fig.12 The RTL Schematic for critical path of S-MB2 recoding scheme

V.CONCLUSION

This methodology is mainly based on the design optimization of FAM operator. By this optimization the performance of arithmetic operations is increased. The fused add multiply design consumes less power than the other existing designs. The proposed sum-modified booth recoder is explored into three different methods by utilizing them in FAM design. There are considerable reductions in critical path latency, utilization of power and area.

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