Volume-4, Issue-5, May Special Issue-2015 • ISSN No 2277 - 8160

Research Paper Engineering

DESIGN OF BIST ENABLED UART USING CELLULAR AUTOMATA LFSR

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ABSTRACT

In today'slife the most manufacturing processes are assure extremely complex including, the manufacturers to con sider testability as a requirement to assure the reliability and the functionality of each of their designed circuits. Most popular test techniques is called Built-In-Self-Test (BIST).It is a design technique that allows a system totest automatically itself with slightly larger system size.A BIST enabledwith UART- Universal AsynchronousReceiver and Transmitter capability will test the UART on chip itself without using external devices. This paper focuses on the TPG (test pattern generator) circuit of BIST, in this paper, the simulation result performance achieved by BIST enabledUART architecture through VHDL programming is enough tocompensate the extra hardware needed in BIST architecture. It generates random test pattern automatically. So BIST takes less test time compared to an externally applied test pattern and helps to achieve much more productivity at the end .

KEYWORDS : VLSI,BIST, UART, VHDL, Cellular automata.

I.INTRODUCTION

Universal Asynchronous Receiver and Transmitter (UART) is a kind of serialcommunication protocol; mostly used for small-distance, less speed, less-cost and the data exchange between computer and peripherals. It is used for asynchronous serial communication by converting data from parallel to serial at transmitter with some extraoverhead busing shift register and vice versa at receiver.

It is generally connected between a processor and peripheral and the processor the UART appears as an 8-bit read/write parallel port. These paper focuses on the design of a UART chip with Enabled BIST architecture using CA(cellular automata) LFSR with the helpof VHDL language.

BIST is a technique to design additional features of hardware and software into ICs to do testing of their own operation using their own circuits,therebyreducing dependence on external Automated Test Equipment (ATE)[6]. BIST is a DesignForTestability technique, because it makes the testing ofa chip easier, faster and less costly, highly efficient. BIST is applicable to any kind of circuit,so its implementation varries the product diversity that it caters to.The rest of paper is as follows. Related Work in section II. Describes the proposed TPG,Section-IV describes the UART, Section-V describes the architecture of UART with BIST, and Section-Videscribes the simulation results and conclusion.

II.LITERATURE SERVEY

There are several technique used to generate test patterns for bist [6], [8], viz. counters, rom,lfsr, cellular automata. a counter can generate an exhaustive but not randomized testsequences[1],[3].drawback of counters as the pattern generator requires more hardware linear Feedback ShiftRegister (LFSR)test pattern generator. These method stores a test patterns compared to previous methods[2],[4].

This normally requires a sequence ofone million pattern in order to achieve high fault coverage[5]. The advantages of LFSR is theircompact and design and currently thepreferred BIST pattern generation [6].

BIST is an on-chip test logic that is utilized to test thefunctional logic of a chip. A generic approach to BIST isshown in below.The BIST solution consists of a Test PatternGenerator and the a circuit to be tested by using bist[2],[3].it is analyze theresults and compress those results for a simplicity and handling. Using With the rapid increase in the design complexity ithas a major design consideration DesignForTestabilityand is becoming incresingly importantanceinSoC[6],[3].Achieving highfault Coverage while maintaining an acceptabledesign overhead and keeping the test time within limits is of importance. BIST help to achieve the required goals. The briefintroductions of BIST architecture component are givenbelow.

Circuit under Test (CUT): It is the portion of the circuittested in BIST mode. It can be sequential and memory . It is delimited by their Primary output andPrimary input[3].

TestPatternGenerator(TPG):TPGgenerates patterns for theCUT. It is a dedicated circuit.Thepatterns may be generate in deterministically[5],[6].

Test response analyser (TRA): These is way to analyse values in sequence on primary output and compares with the expected output[3].

BIST Controller Unit (BCU): It controls the test execution, itmanages the TRA,TPG and reconfigures the multiplexer and CUT[6].

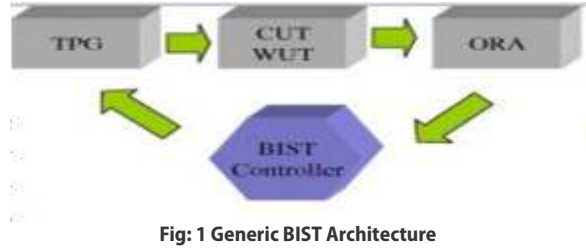


Fig: 1 Generic BIST Architecture

III.PROPOSED TPG

In previous design normal LFSR design used in TPG circuit,But proposed design consist the Cellular Automata LFSR is used.

CA LFSR

Cellular Automata (CA) consists of a collection of cells/nodes formed by flip-flops which are logically related to their nearest neighbors using XOR gates [2] [4]. When the value of a node is deter-mined only by two neighboring cells the CA is known as one-dimensional linear CA (for the rest of the text one-dimensional linear CA is referred as CA). The logical relations which relate a node to its neighbors are known as rules and they de-fine the characteristics of a CA. There are many rules which can be used to construct a CA register, the most popular being rules 90 illustrated in Figure.

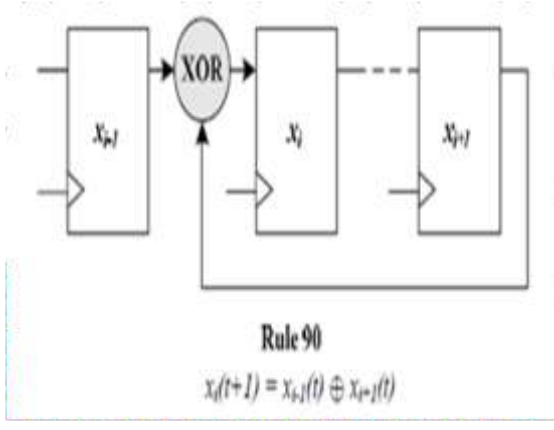


Fig:2 CA rule 90

The CA LFSR is designed by using CA rule 90, which generate the random values in TPG for UART, the CA LFSR is shown in figure 3.

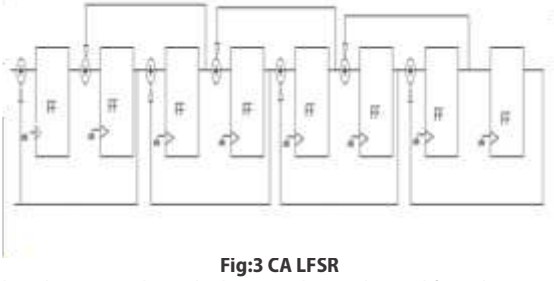


Fig:3 CA LFSR

When the trg signal goes high, a new data is obtained from the CA LFSR which is fed in parallel to the input of the transmitter and the calfsr output is given to PISO (parallel in serial out) block in TPG, it generates the serial data to UART receiver input. The complete TPG block is shows in figure.

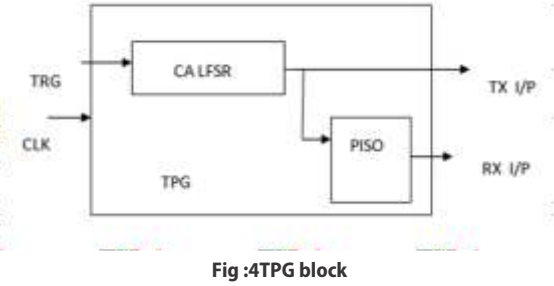


Fig :4TPG block

IV.UART

Universal asynchronous receive transmit (UART) is an asynchronous serial receiver/transmitter. It is a piece of computer hardware that commonly used in PC serial port to translate data between parallel and serial interfaces. The UART takes bytes of data and transmits the individual bits in a sequentialoneTheUART re-assembles the data into eight bits. Thus, the transmitter and receiver must agree on timing parameters in advance and special bits are added to each word. It is used to synchronize the transmitting and receiving units. In general, UART contains of two main block, the transmitter and receiver block.

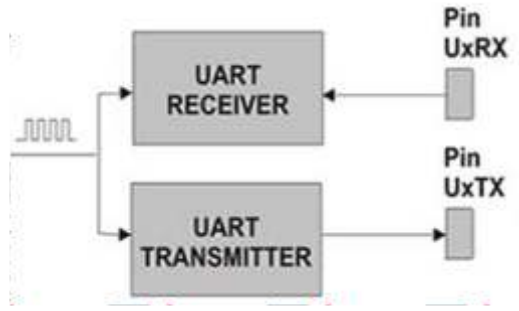


Fig:5UART Blocks

A.UART TRANSMITTER SECTION

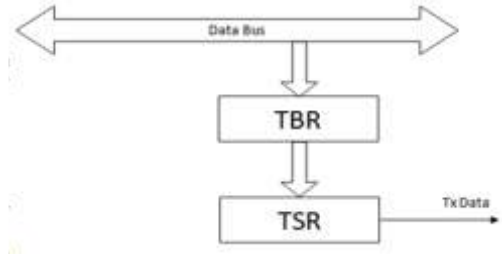


Fig:6UART Transmitter

The Block diagram of UART Transmitter is as shown in figure.The data is loaded from Data Bus into TBR (Transmit Buffer Register) and from TBR to TSR (Transmit Shift Register), based on the control and status signals produced by the Control unit. The Size of TSR is taken in such a way that, it should accommodate the START and STOP bits along with the Data bits which are loaded from the Data bus.

B.UART RECEIVER SECTION

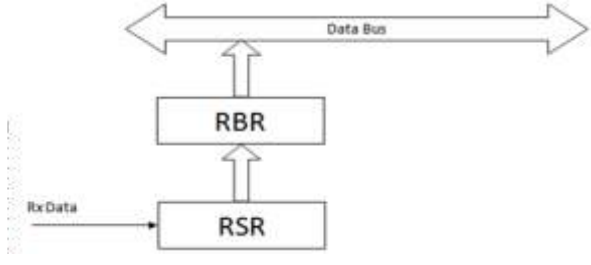


Fig:7UARTreceiver

The block diagram of UART Receiver is as shown in figure.7 The data receiving will be captured using receiving baud clock and then loaded into RSR (Receive Shift Register) and from RSR to RBR (Receive Buffer Register), and then to Data Bus, based on the control and status signals produced by the Control unit. The Size of RSR is taken in such a way that, it should accommodate the START and STOP bits along with the Data bits which are loaded from the Data Bus.

V.UART BIST DESIG

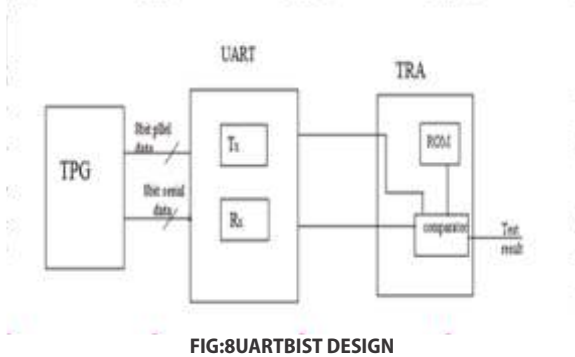


FIG:8UARTBIST DESIGN

When the trigger signal goes high then only a new value is generated in the LFSR. This LFSR will generate (28-1) different pseudorandom values,. The parallel output "TX i/p" is fed to the transmitter and the serial output is fed to the receiver section of the UART.

When the trg signal goes high, a new data is obtained from the LFSR which is fed in parallel to the input of the transmitter. After a certain number of clock cycles, the same data is obtained at the output of the transmitter as serial data. This serial data is shifted in the SIPO of the comparator and this is the sipo_op data. This sipo_op is compared with the ROM data (romd). The shaded regions in the figure shows the time of comparison. Depending on the comparison, the result (i.e. rslt) is generated. If the both sipo_op and romd are same then rslt=1,elserslt=0.

As the receiver provides 8-bit parallel output, a SIPO is not required.The output from the receiver "rop" is directly compared with romd. The shaded regions in the figures showat comparison time. In all the shaded regions, except the last one romd and rop are same and so the rslt is 1 in all those cases. But in the last comparison, due to the intentionally stored incorrect data in the ROM the comparativeresults inrslt=0. Henceforth comparison procedure is stopped and the CUT is announced to be faulty.

ROM

ROM is used to store the 8-bit pseudo random patterns, in order, that will be obtained as the output from the Transmitter and Receiver sections of the developed UART. The data that are obtained as the outputs of the receiver and the transmitter are compared with the data stored at the corresponding addresses of the ROM by the comparator which verifies whether the CUT is working properly or not.

VI.SIMULATION RESULT

BIST Enabled UART result



Fig:8 BIST enabled uart

TPG results

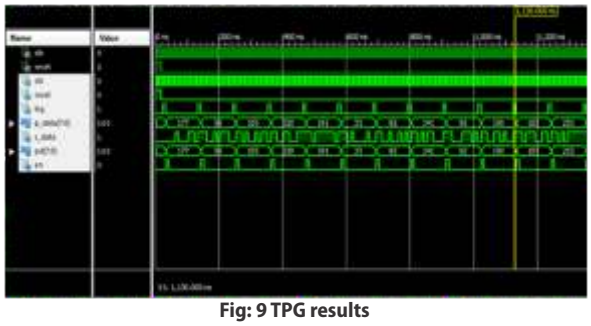


Fig: 9 TPG results

UART RESULTS



Fig:10 uartresult



Fig:11 TRA results

VII.CONCLUSION

This paper implements the BIST Enabled UART with cellular automata LFSR as TPG and total design Using VHDL language, enabled BIST test the UART transmitter and receiver modules by comparing both outputs at TRA units.

Its performance checked by comparatorCompared to excepted results stored in ROM. The BIST has two types,logical BISTAnd memory BIST,MBIST has more advantages compared to LBIST, but reduced developlement efforts, at high speed tests, no external test equipment.

The improvement can be in the field implementation of CALFSR.rather than LFSR.less feedback required in cellular auto mata lfsr,less time ,more effiency.

These simulation results shown in paper. BIST enabled UART using CALFSR is Working vey well.The hardware test by using FPGA(spartan3E).

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