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Development of IP Core for Viterbi Decoder using VHDL

Hiral Pujara — Electronics and Communication Engg. Department, GTU L. D. College of Engineering, Ahmedabad- 380015, India

Pankaj P. Prajapati — Asst. Prof, Electronics and Communication Engg. Department, GTU L. D. College of Engineering, Ahmedabad- 380015, India

ABSTRACT

Forward Error Correction techniques are utilized for correction of errors at the receiver end. Convolutional encoding is an FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by additive white Gaussian noise (AWGN). Viterbi algorithm is a well known Maximum-likelihood algorithm for decoding of Convolutional codes. They have rather good correcting capability and perform well even on very noisy channels. It has been widely deployed in many wireless communication systems to improve the limited capacity of the communication channels. Although widely-used, the most popular communications decoding algorithm, the Viterbi algorithm, requires an exponential increase in hardware complexity to achieve greater decode accuracy. The main Objective of this paper is to analyze impact of constraint Length on the performance of proposed Viterbi Decoder Design. In this paper, resource optimized Viterbi Decoder with rate ½ and Constraint length 3 as well as 4 has been designed using Trace back architecture. The proposed Viterbi Decoder has been designed using VHDL, simulated using Xilinx ISE Simulator and synthesized with Xilinx Synthesis Tool (XST). The comparative analysis between two constraint lengths is done then simulated and synthesized result shows that as constraint length increases there is an increase in hardware complexity and reduction in Max. Frequency. The Viterbi Decoder is compatible with many common standards, such as DVB, 3GPP2, 3GPP, IEEE 802.16 and LTE.

KEYWORDS : Convolutional Encoder, Viterbi Algorithm, Viterbi Decoder, Forward Error Correction (FEC), Traceback method

I. Introduction

Encoding the information sequence prior to transmission implies adding extra redundancy to it, which is then used at the receiver end to reconstruct the original sequence, effectively reducing the probability of errors induced by a noisy channel. Different structures of codes have developed since, which are known as channel coding. The encoder adds redundant bits to the sender's bit stream to create a codeword. The decoder uses the redundant bits to detect and/or correct as many bit errors as the particular error control code will allow. Like any error correcting code, a Convolutional code works by adding some structured redundant information to the user's data and then correcting errors using this information. There have been a few Convolutional decoding methods such as sequential and Viterbi decoding, of which the most commonly employed technique is the Viterbi Algorithm (VA).

Viterbi decoding was developed by Andrew. J. Viterbi, the founder of Qualcomm Corporation in April, 1967 [18]. Viterbi algorithm is being widely used in many wireless and mobile communication systems for optimal decoding of Convolutional codes. The Viterbi alignment is a dynamic programming algorithm for finding the most likely sequence of hidden states – called the Viterbi path – that results in a sequence of observed events, especially in the context of Markov information sources and hidden Markov models. Applications using Viterbi decoding [9] include digital modems and digital cellular telephone, where low latency, component cost and power consumption are must.

Ii Viterbi Decoder

Figure 1 shows Basic Block Diagram of Convolution Encoding and decoding which basically consists three main blocks: Convolutional Encoder, AWGN Channel and Viterbi Decoder.

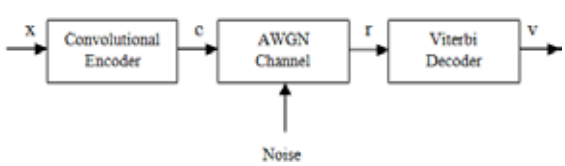


Fig. 1 Block Diagram of Convolution Encoding and Decoding

A. Convolutional Encoder

In convolutional encoding n-tuple of data is generated for every k-tuple of inputs based on both current and K-1 previous k-tuples where K is called constraint length of the code. A (n, k, m) convolutional code can be implemented with a k-input, n-output linear sequential circuit with input memory 'm'. Typically, 'n' and 'k' are small integers with k<n, but the memory order 'm' must be made large to achieve low error probabilities. The constraint length K of the code represents the number of bits in the encoder memory that effect the generation of the n output bits and is defined as K = m+1.. The code rate r of the code is a measure of the code efficiency and is defines as r= k/n.

The proposed Encoder has the following specifications given below and schematic shown in Figure 2.

Constraint Length: K = 3, Input bit: k = 1, Output bit: n = 2 Generator Polynomials: $G1 = 1 + X + X^2$, $G2 = 1 + X^2$

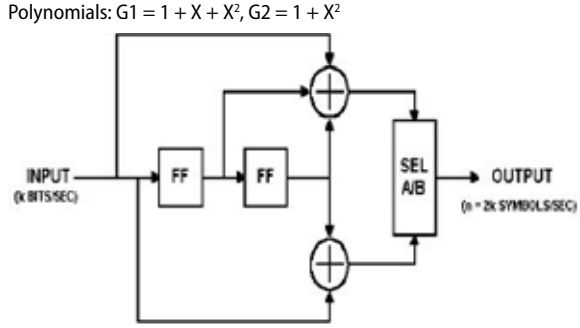


Fig. 2 Convlolutional Encoder (Rate ½, K = 3)

For Constraint Length: K = 4 and Rate ½ Generator Polynomials are [1]: $G1 = 1 + X + X^2 + X^3$, $G2 = 1 + X + X^3$

B. Viterbi Decoder

Error correction is an integral part of any communication system and for this purpose, the convolution codes are widely used as forward error correction codes. . The two decoding algorithms used for decoding the Convolutional codes are Viterbi algorithm and Sequential algorithm. Sequential decoding has advantage that it can perform very well with long constraint length Convolutional codes, but it has a variable decoding time. Viterbi decoding is the best technique for decoding the Convolutional codes but it is limited to smaller constraint lengths (K<10) [2]. It has fixed decoding time compared to sequential decoding. With the Viterbi algorithm, storage and computational complexity are proportional to 2^K.

A Viterbi algorithm consists of the three major parts [15]: Branch metric unit, Path metric unit and trace back as shown in Figure 3.

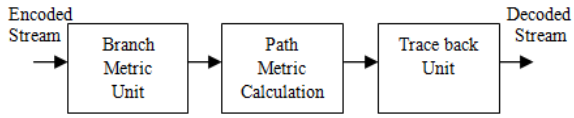


Fig. 3 Block Diagram of Viterbi Decoder [10]

1) Branch metric calculation
The first unit is called Branch metric unit. The Hamming distance (or other metric) values we compute at each time instant for the paths between the states at the previous time instant and the states at the current time instant are called branch metrics. Hamming distance or Euclidean distance is used for branch metric computation.

2) Path metric calculation
An accumulated Error metric called path metric (PM) contains the 2^{K-1} optimal paths. The current Branch Metric is added to previous PM and each the two distances are compared for all Add- compare select unit

In terms of speed the performance of Viterbi Decoder is mainly determined by the number of ACS (2^{K-1}) units and their computation time. As shown in figure each ACS unit comprises two adder blocks, a comparator and a selector block.

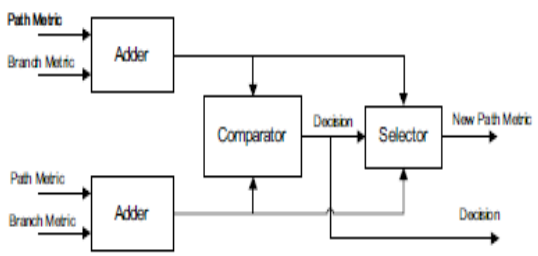


Fig. 4 Block Diagram of Add Compare Select unit [9]

3) Trace back unit
The final unit is trace back unit where the survivor path and output data are identified. The Viterbi decoding flowchart is given in Figure 5.

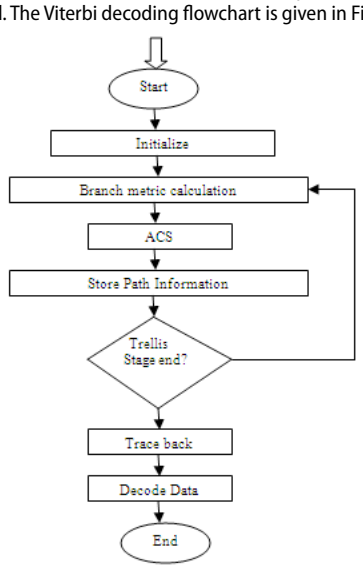


Fig. 5 Viterbi decoding Flow Chart

C. Types Of Viterbi Decoding

There are two types of Viterbi Decoding: Hard Decision Viterbi Decoding and Soft- Decision Viterbi Decoding.

1) Hard decision Viterbi deocding
Demodulator output configured by variety of ways [1]: In which output of demodulator is quantized into two levels, zeros and one and fed into decoder. Decoder operates on hard-decisions made by demodulator, decoding is called Hard- decision decoding. In which path through trellis is determined using hamming distance measure.

2) Soft decision Viterbi deocding
In which output of demodulator is quantized into greater than two levels [1]. If output of demodulator is quantized into 3-bit result in 8-level output then 3-bits is used to describe each code symbol. In which Euclidian distance as a distance is measured instead of hamming distance. The advantage of using soft- decision decoding is to provide decoder with more information, which decoder then use for recovering the message sequences. It provides better error performance than hard- decision type Viterbi decoding. Disadvantage of using soft decision decoding is increase in required memory size at decoder and reduce speed.

D. Viterbi Decoding Techniques

There are mainly two types of decoding techniques available in order to decode the data at the receiver end.

1) Register Exchange Method
In this method, a register assigned to each state contains information bits for the survivor path from the initial state to current state. In fact, register keeps decoded output sequences along the path. This method requires copy of all registers at each stage. The need to trace back is eliminated since the register of final state contains decoded output sequence. This approach results in complex hardware due to need to copy contents of all register in a stage to next stage. Since the RE method does not need tracing back, it is faster.

2) Traceback Method
Trace back is memory organization method to store survivor paths and retrieve the decoded data. Direct implementation of this method is not practical because of an infinite storage size is needed; therefore in practice semiconductor infinite memory locations are reused periodically. The Trace Back Unit performs three operations: write new Data, Trace Back Read and Decode Read. Memory is organized as a two dimensional structure where row are assigned to states and columns to time steps. Three memory blocks are used in operation: write block is used to store ACS decision vectors, Decode block where the decoded bit sequences is read in backward order and Trace Back Block which is used to find the starting point of next trance back sequences. Traceback Depth (D) is a predefined parameter that defines the size of each memory block [15]. Traceback method is area efficient and better than RE method. .Register exchange method requires complex hardware compare to the Traceback method for larger constraint length though it will give faster speed.

In this project, I had implemented a hard decision and trace back method for Viterbi decoding. The design Entry done using Xilinx ISE 10.1 Design suite.

iii Simulation And Synthesis Results
Synthesis is a process of constructing a gate level netlist from a register transfer level model of a circuit described in Verilog HDL. Increasing design size and complexity, as well as improvements in design synthesis and simulation tools, have made Hardware Description Languages (HDLs) the preferred design languages of most integrated circuit designers. The two leading HDL synthesis and simulation languages are Verilog and VHDL. Both have been adopted as IEEE standards.

A. Simulation Waveforms of Viterbi Decoder

The Simulation Waveform of Viterbi Decoder is shown in Figure 6 (For Rate ½ and K = 3) and Figure 7 (For Rate ½ and K = 4). To observe the speed and resource utilization, RTL is generated, verified and synthesized using Xilinx Synthesis Tool (XST).

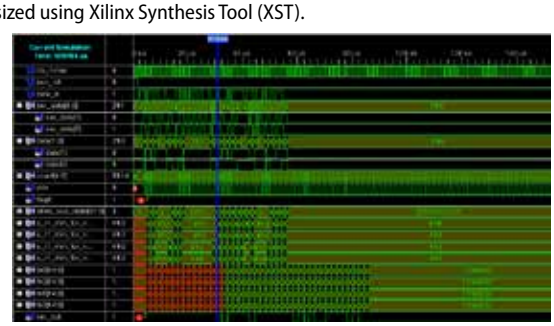


Fig. 6 Simulation Waveform of Viterbi Decoder (Rate ½, K =3)

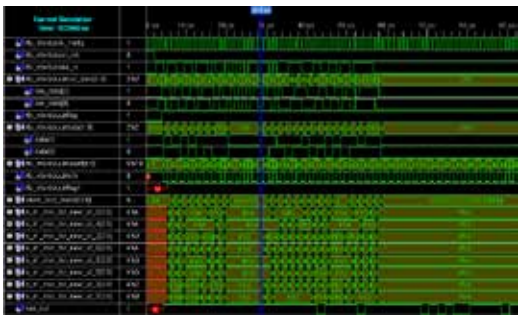


Fig. 7 Simulation Waveform of Viterbi Decoder (Rate ½, K = 4)

B. RTL Schematic of Viterbi Decoder

Below Shown is the RTL Schematic of the Viterbi Decoder.



Fig 8 RTL Schematic of Viterbi Decoder

B. Device Utilization Report

This synthesis report is generated after the compilation of Design for the targeted Xilinx SPARTAN 3A based Xc3s400a FPGA Device. Here, The Design unit is not implemented on targeted FPGA Device. This report contains about component used and also Timing and power summary.

Table 1. Comparative Analysis between two constraints Length

Device Utilization Summary (xc3s400a-4ft256)		
	Rate ½, K = 3 G1: (1,1,1), G2: (1,0,1),D = 5K =15	Rate ½, K = 4 G1: (1,1,1,1), G2: (1,0,1,1) D = 5K = 20
Logic Utilization	Used/Available	Used/Available
Number of Slices	104/3584	261/3584
Number of Slice FFs	95/7168	215/7168
Number of 4 input LUTs	146/7168	363/7168
Number of Bonded IOBs	4/195	4/195
Number of GCLKs	2/24	2/24
Timing Summary (xc3s400a-4ft256)		
Min. Period	30.190ns	69.478ns
Max. Frequency	33.124MHz	14.393MHz
Minimum input arrival time before clock	2.993ns	3.025ns
Maximum output required time after clock	5.531ns	5.531ns
Power Summary (xc3s400a-4ft256)		
Power consumption: P (mw):	49 mw	49 mw

IV Conclusions

In this Paper Resource optimized Viterbi Decoder with rate ½ and constraint length 3 as well as 4 has been proposed. The proposed Viterbi Decoder has been designed with VHDL using traceback method. The designed Viterbi Decoder has been simulated using Xilinx ISE simulator and synthesized with XST. The simulated and synthesized results show that proposed design can work at an estimated frequency of 33.124 MHz and 14.393 MHz for constraint length 3and 4 respectively by using considerable less resources of target FPGA device SPARTAN 3A. This Paper also shows impact of constraint length on the performance. The comparative analysis result shows that as constraint length increases VLSI hardware complexity increases and Max. Frequency decreases.

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