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EFFICIENT FIXED POINT LMS ADAPTIVEFILTER IMPLEMENTATIONONFPGA

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ABSTRACT

The main purpose of DLMS Adaptive filteris to reduce the power and time complexity. By using partialproduct generator we can achieve low area- delay- power andadaptation delay. DLMS is used to develop an efficientarchitecture,it is most popular for real-time adaptive system.The present system is found tobe more systematic in termsof power and energy delay product comparedto the previous system.The present system offers nearly17% fewer area-delay product(ADP) and 14% fewer energydelay product(EDP)than the previous system, for filter lengthN=8,16,and32.By using pruning in the proposed system we canprovide 20% saving in ADP and 9% saving in EDP .An efficientfixed point implementation scheme is implemented in the proposedsystem.

KEYWORDS : Adder, DLMS Adaptive Filter, Weight Update Block

I. INTRODUCTION

A filter is an important component in the communication world. Mainly, it eliminates the unwanted signal from the function of thesystem. Adaptivefilter[1] is the filter mostly used in the digital signal processing area. A famous Widrow-Hoff-least-mean-square algorithmmay be considered as the one of simple know adaptive filter. One of the most popular adaptive filter is LMS adaptive filter[2] . Itspopularity is due to its low complexity as well as its stability and satisfactory convergence performance. LMS algorithm does not supportpipelined implementation .so that it may be modified as delayed LMS algorithm[5][6].whereas it allows pipe lined implementation of the filter .pipelined architectureis the operation where if one operation is going on then the required output isstored in the register lly the next operation will start to perform the operation.For increasing particular frequency of the systolic architecture[7][10] in the DLMS algorithm have to be implement a heavy work. Adaptive filter is the most commonly used in the algorithm such as LMS algorithm, due to its extraperformanceand simple calculations.

II.EXISTING SYSTEM

The existing system on the DLMS adaptive filter doesn't implementthe fixed point implementation scheme. The structure of the DLMSadaptive filter is as shown in the figure 1.

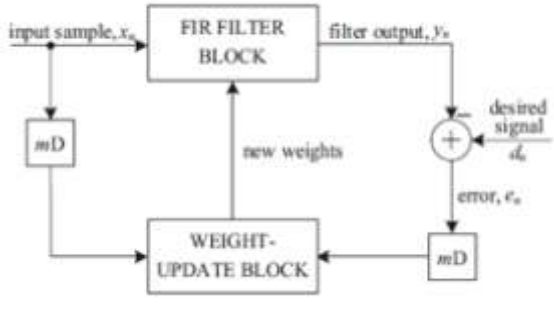


Figure 1Structure of the existing delayed LMS adaptive filter

Here the adaption delay of m cycleamounts to the delay introduced by the complete adaptive filter structureconsists of FIR filtering and weight update process.now this existing system LMS can be decomposed in to the two partsfirst part is the delay introduced by the conduit stages in FIR filter andother part of the delay is the weight update block. A DLMS adaptivefilter can be accomplishment by a structure a shown in the figure.

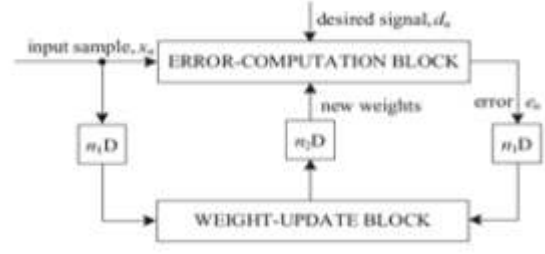


Figure 2 Structure of modified DLMS adaptive filter

A modified algorithm can be ramify in to two blocks.It performs the conduit by feed forwardcut-set retiming to decrease the no of conduit stages and adaptationdelay[3][4]. In present DLMS delay get minimized due to the pipe linedstructure. The delay is high in previous system due to usabilityof the systolic architecture.

III.PROPOSED SYSTEM

A DLMS adaptive filter is said to be consists of two blocks.They are
1.Error Computation Block
2. Weight Update Block.

1.ErrorComputationBlock

It consists of an n-tap DLMS adaptive filter as show in the figure.

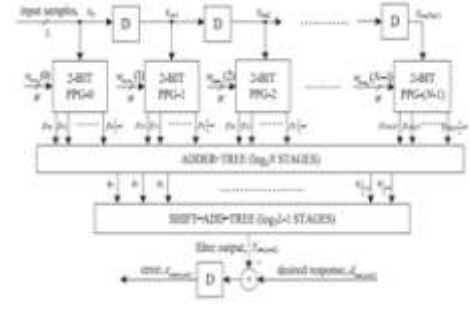


Figure 3 Structure of error computation block

Where it consists of n number of 2 bit PPG corresponding to n multiplier and clusters of L/2 binary adder tree, followed by a single shift adder tree .It maybe explained by the sub block in details.

a) StructureofPPG

The structure of PPG is said to be a shown in the figure .It consists of 2 to 3 decoder of L/2 number and equal to the number of and/or cells.A2 to3 decoder takes 2 bit digit as input and produces 3output.The output produced by the decoder such as b0,b1,b2 along with w,2w,3w are given as input to the AOC. where w,2w,3w are in 2's complement representation.

b)StructureofAOC's

An AOC consists of 3 and cells and 2 or cells .Each and cell contains n-bit input and single bit input b of n and gates. The input D of n bit of and gate are fed as one of input and the other input of n and and gate are fed as input b .The output of AOC is w,2w,3w there are similar corresponds to the decimal values of 1,2,3.The 2 bit multiplication is performed by AOC along with the decoder.

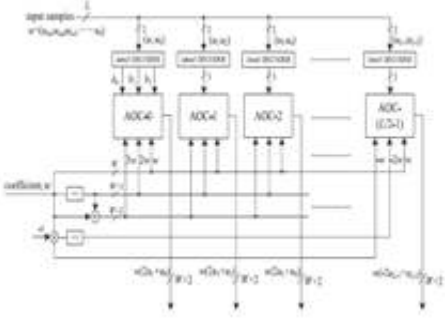


Figure 4 Structure of PPG and AOC cell

c)Fixed Point Considerations

To reduce the hardware complexity without the degradation of steady state MSE, The fixed-point implementation[9] of the proposed DLMS adaptive filter shows the bit level pruning of the adder tree.In fixed-point implementation,for input samples, weights, and internal signals the word lengths and radix points are need to be decided. Fig. shows the Fixed-point representation of a binary number. Table1shows the fixed-representation of the desired signals; its quantization is usually given as an input.

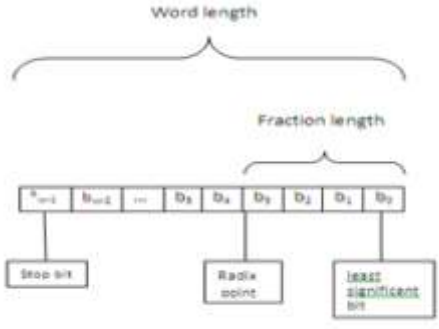


Figure 5 Fixed point implementation of binary number

Signal Name	*Fixed-Point Representation*
X	(L, L_i)
W	(w, w_i)
P	$(w+2, w_i+2)$
Q	$(w + 2 + \log_2 N , w_i +2 + \log_2 N)$
y,d,e	$(w, w_i + L_i + \log_2 N)$
μe	(w, w_i)
R	$(w+2, w_i+2)$
S	(w, w_i)

Table 1 Fixed point representation of DLMS adaptive filter

d)Adder Tree Optimization

The adder and shift–add tree computation can even up for compression of area, delay,[8]and power complexity. To reduce the computation entanglement the inputs of the adder tree can be diminished and the ward pard can be used to reduce the impact of shorten on the fallacy performance of the adaptive filter. To have more tackle saving, the bits to be diminished are not generated by the PPGs, so the complexity of PPGs also gets reduced.

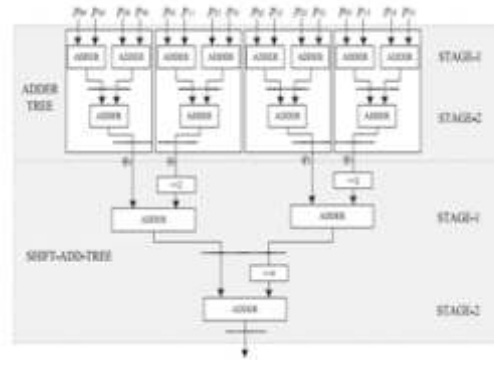


Figure 6Adder structure of filter for N=4,L=8

2.Weight-Update block:

The proposed structure of weight-update block is shown in Fig.7. It performs N multiply-accumulate operations of the form $(\mu \times e) \times x_i + w_i$ to update N filter weights. The step size μ is taken as a negative power of 2 to realize the multiplication with recently available error by the shift operation. Each MAC unit performs the multiplication of the shifted value of error with the delayed input samples xi followed by the additions with the corresponding old weight values w_i.

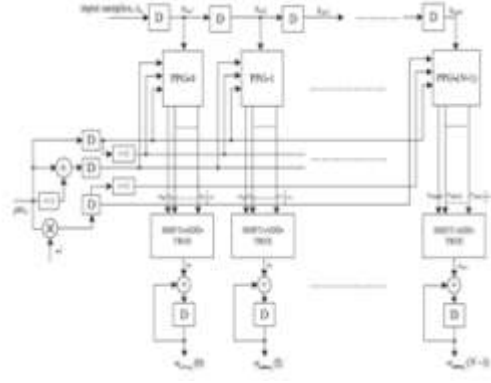


Figure 7 Structure of weight update block

IV RESULT

The design is stimulated in xilinx software and developed in VERILOG language as shown in the figure.

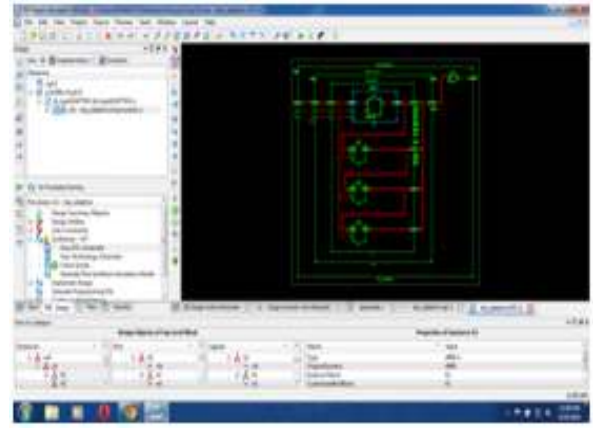


Figure 8 Existing RTL Schematic

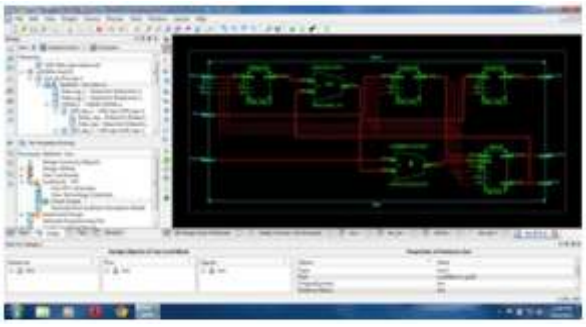


Figure 9 Proposed RTL Schematic

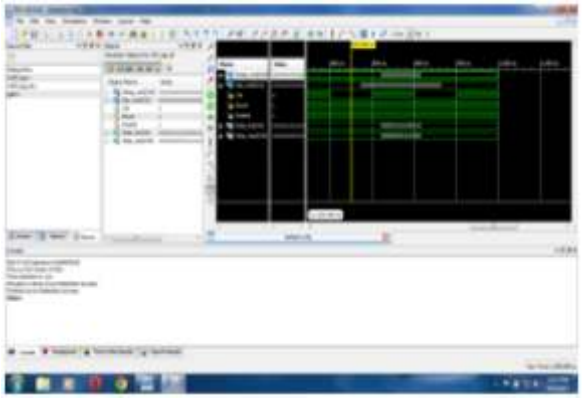


Figure 10 Existing Output Waveform



Figure 11Proposed Output Waveform

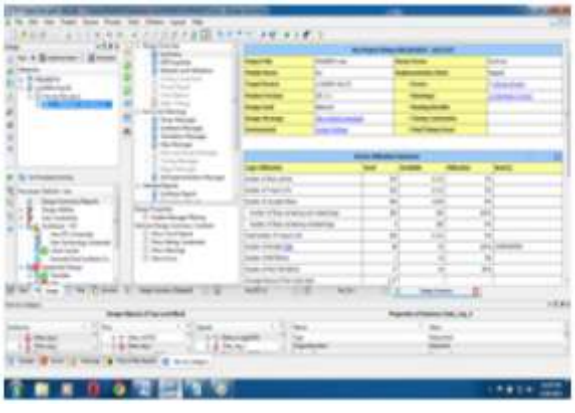


Figure 12 Device Utilization Summary(Area) Of Existing System

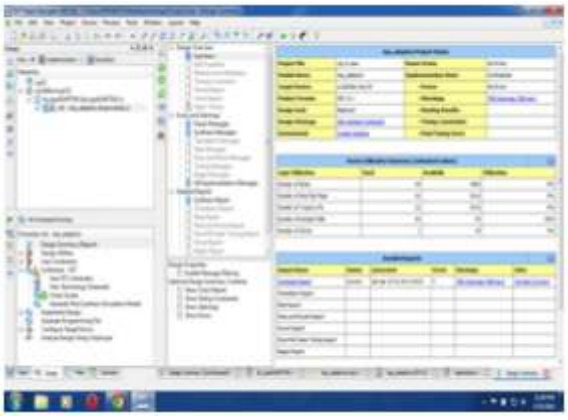


Figure 13 Device Utilization Summary (Area) Of Proposed System



Figure 14 Delay And Speed Summary Of Existing System



Figure 15 Delay And Speed Summary Of Proposed System

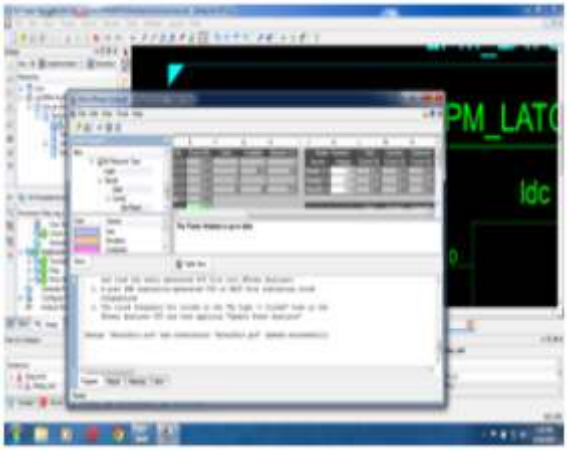


Figure16power summary of existing system



Figure 17 Power Summary of Proposed System

V CONCLUSION

Compare to the existing system, the proposed system offers less adaptation delay. It provides significantly saving of ADP and EDP compared to previous system. Adaptive filter requires to operate at a lower sampling rate. By lowering the operating voltages it reduces the power further.

REFERENCES

(1)B. Widrow and S. D. Stearns, Adaptive Signal Processing. EnglewoodCliffs, NJ, USA: Prentice-Hall, 1985|| (2) S. Haykin and B. Widrow, Least-Mean-Square Adaptive Filters. Hoboken,NJ, USA: Wiley, 2003|| (3) S.Ramanathan and V.Visvanathan, "A systolic architecture for LMS adaptive filtering with minimal adaptaiondelay,"in proc. Intconf very large scale integer,(vlsi) design,jan. 1996,pp. 286-289|| (4)L.D.Van and W.S.Feng, "an efficient systolicarchitecture for the DLMS adaptive filter and its applications," IEEEtrans. Circuits syst. Ii, analog digital signal process., vol. 48, no. 4, pp. 359–366, apr. 2001.|| (5) G. Long, F. Ling, and J. G. Proakis, "Corrections to 'The LMS algorithmwith delayed coefficient adaptation,"' IEEE Trans. Signal Process.,vol. 40, no. 1, pp. 230–232, Jan. 1992.|| (6) M. D. Meyer and D. P. Agrawal, "A modular pipelined implementationof a delayed LMS transversal adaptive filter," in Proc. IEEE Int. SympCircuits Syst., May 1990, pp. 1943–1946|| (7) H. Herzberg and R. Haimi-cohen "A systolic array realization of anLMS adaptive filter and the effects of delayed adaptaion", IEEE trans. Signalprocess., vol. 40, no. 11, pp.2799 -2803 1992|| (8)P. K. Meher and S.Y. Park "low adaptation-delay LMS adaptive filterpart-ii: an optimized architecture", proc. IEEE int. Midwest symp. Circuitssyst., pp.1 -4 2011|| (9) R. Rocher , D. Menard , O. Sentieys and P. Scalart "Accuracy evaluation of fixed-point a LMS algorithm", proc. IEEE int. Conf.acoust., speech, signal process., pp.237 -240 200|| (10)H.Herzberg and H.Haimi-cohen, "A systolic array realization of an LMS adaptive filter and the effects of delayed adaptation", IEEE trans. Signalprocess., vol. 40, no. 11, pp.2799 -2803 1992.