Volume-4, Issue-5, May Special Issue-2015 • ISSN No 2277 - 8160

Research Paper Engineering

Fully Reused VLSI ArchitectureOf FMO/Manchester Encoding Using SOLS Technique For DSRC Applications

Shaik.Kamila Department of Electronics and Communication Engineering Narayana Engineering College,Nellore-524003, A.P, India

M.praveenKumar Department of Electronics and Communication Engineering Narayana Engineering College,Nellore-524003, A.P, India

ABSTRACT

An emergingtechnique is DSRC (dedicated short range communication) that force the good transportation system into our day to day life. This DSRC standard taken on Manchester and fmo codes to achieve dc-balance, raising the reliability of signal. Nonetheless, the code diversity between the Manchester and fmo coding gravely limits the potential to design a reused VLSI architecture for both coding technique The proposed technique is similarity oriented logic simplification techniques to overtake this limitation.

The SOLStechnique develops the hardware utilization rate from 57.14% to 99.2% for FM0/Manchester encodings. The fmo and Manchester encoding has maximum operation frequency is 2 GHz and 900 MHz, respectively. The power consumption of fmo encoding is 1.14mW at 900MHz and Manchester encoding is 1.58Mw at 2GHz

KEYWORDS : Dedicated short-range communication (DSRC),Flexible macro block ordering (fmo) encodingand Manchester encoding, VLSI

I. Introduction

DSRC(dedicated short range communication) [1] is a protocol used for communication for a short range of distance, say a few hundred meters through a dedicated channel. It is used to introduce intelligent transport service into our day to day life. The DSRC communication aids in both automobile-to-automobile as well as automobile-to-roadside. In automobile-to-automobile, the DSRC enables the messagesending and broadcasting among automobiles for safety issues and public information announcement [2]. The safety issues include blind-spot, intersection warning, intercars distance, collision-alarm and hard break warning etc[3]. The automobile-to-roadside Concentrate on the intelligent transportation service, such as, mainly deals with the collision alarms, hard Electronic Toll Collection (ETC), railway intersection warning, in vehicle signing etc.

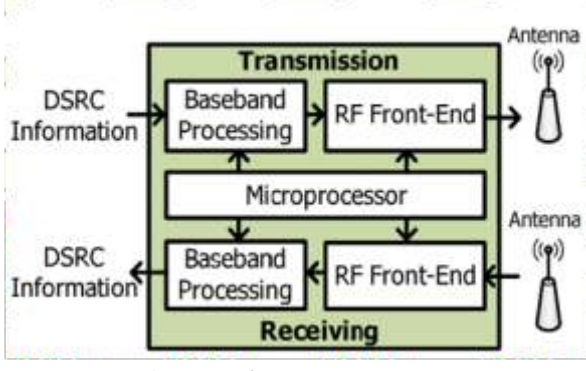


Fig.1.System Architecture of DSRCtransceiver.

In additional, it also supports in smooth traffic control. The three equipment Method are used namely; themicroprocessors, RF front end and base band processors which is shows in fig [1].The micro processor interprets instructions from media access control to schedulethe tasks of baseband processing and RF front-end. The baseband processingis responsible for modulation, error corrections, clock synchronization, and encoding. The RF frontend transmits and receives the wireless signal through theantenna

Finally an impotent function is the base band processing consists of error correction, modulation, clock synchronization, and encoding. The aim of data encoding is an FM0 or Manchester encoding are used so as to decrease the noise in the channel when it is left idle. When Fmo and Manchester encoding is fulfilled then, reducing the hardware utilization rate and also reducing the efficiency. That impact on system performance. Therefore a new method is introduced to increase the hardware utilization rate i.e., The Similarity Oriented Logic Simplification (SOLS) method of reusable architecture thereby increasing the performance and area footage

II.Literature survey

The literature [4] proposes a VLSI architecture of Manchester encoder for optical communications. This design adopts the CMOS inverter and the gated inverter as the switch to construct Manchester encoder. It is implemented by0.35-μm CMOS technology and its operation frequency is 1 GHz. The literature [5] further replaces the architecture of switch in [4] by the nMOS device. It is realized in 90-nmCMOS technology and the maximum operation frequency is as high as 5 GHz. The literature [6] develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) Applications. This design is realized in 0.35-μm CMOS technology and the maximum operation frequency is 200 MHz.

III. Related Technique

I. DSRC Protocal

Dedicated short-range communication (DSRC) is a fast, short to mid range, wireless technology. It is one way or two way communication between vehicles or between vehicles and roadside. It is used to make travel easier and minimizes the impact vehicles have on the environment. It provides vehicles and infrastructure the ability to communicate with each other at a rate of 10 times per

. The most important concern of dsrc is communication is collision detection. Each DSRC fitted for vehicle broadcasts its including speed, trajectory, location etc to a short range of distance, say a few hundred meters.

II. Methodology

a. FM0 Encoding

The coding principle of FM0 is listed as the following three rules.

1) If X is the logic-0, the FM0 code must exhibit a transition between A and B.

2) If X is the logic-1, no transition is allowed between A and B.

3) The transition is allocated among each FM0 code no matter what the X is.

A FM0 coding example is shown in Fig. 2. At cycle 1, the X is logic-0; therefore, a transition occurs on its FM0 code, according to rule 1. For simplicity, this transition is initially set from logic-0 to -1. According to rule 3, a transition is allocated

Fig. 2.FM0 encoding

Among each FM0 code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the X of logic-1.Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

Fig.3.FMO Encoder

a. Manchester Encoding

This encoding example is given in fig4. The Manchester code is gained from

$X \oplus CLK \ldots$ (1)

The XOR operation performs the Manchester encoding for CLK and X. The transition of clock is always within one cycle and so does the Manchester code nothing about what the X is.

Fig. 4.Manchester Encoding

The XOR gate is used to implement the Manchester encoding where the clock and data signals are XORed together to obtain the encoded data as shown in below fig.5.

Fig.5. Manchester Encoding

III.Limitation Analysis on Hardware Utilizationsof FM0 Encoder and Manchester Encoder

To make an analysis on hardware utilization of FM0 and Manchester encoders, the hardware architectures of both areconducted first. As mentioned earlier, the hardware architectureof Manchester encoding is as simple as a XOR operation.However, the conduction of hardware architecture for FM0is not as simple as that of Manchester. How to construct thehardware architecture of FM0 encoding should start with theFSM of FM0 first. In Fig. 6(a)shows, the FSM of FM0 code is separated into four states. A state code is individually allotted to each state, and each state code lies in A and B, as given in Fig. 2. According to the coding principle of FM0, Fig. 6(b) shows FSM of FMO code. Imagine the first state is S1, and its state code is 11 for A and B, respectively. whenX is logic-0 that is S3, the state-transition must proceed withboth rules 1 and 3. The next-state can only satisfies both rules for the X of logic-1 is S4v Thus, the state-transition of each state can be completely constructed

fig6(a). States definition

Fig6 (b) FSM of Fm0.

The FSM of FM0 transition table is

TABLE II
TRANSITION TABLE Of FM0

Previous-state		Current-state			
		A(t)		B(t)	
A(t−1)	B(t−1)	X = 0	X = 1	X = 0	X = 1
1	1	0	0	1	0
1	0	1	1	0	1
0	1	0	0	1	0
0	0	1	1	0	1

A(t) and *B(t)* is a discrete-time state code of current-state at time instant. Their previous-states are *A(t* 1*)* and *B(t* 1*)*.the Boolean functions of *A(t)* and *B(t)* are given as

$A(t) = B(t-1)$…. (2)

$B(t) = X \oplus B(t-1)$….. (3)

With both A (t) and B(t), the Boolean function of FM0 code is denoted as

$CLKA(t) + CLKB(t)$…..(4)

With (1) and (4), the hardware architectures of FM0 and Manchester encoders are shown in Fig. 7. the Manchester encoder is as simple as a XOR operation for *X* and CLK. Nevertheless, the FM0 encoding depends not only on the *X* but also on the previous-state of the FM0 code. The DFF*A* and DFF*B* store the state code of the FM0 code. The MUX−1 is to switch *A(t)* and *B(t)* through the selection of CLK signal. Both *A(t)* and *B(t)* are realized by(2)and (3), respectively. The determination of which coding is adopted depends on the Mode selection of the MUX−2, where the Mode = 0 is for FM0 code, and the Mode = 1 is for Manchester code. To evaluate the

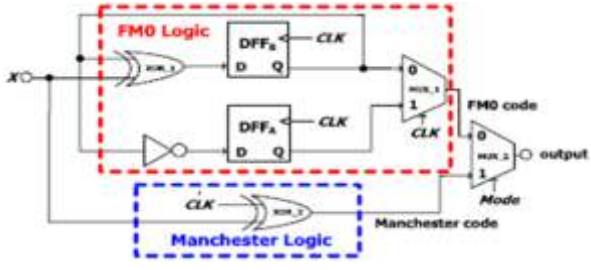


Fig7. Hardware architecture of FM0 and Manchester encodings

hardware utilization, the hardware utilization rate (HUR) is defined as

HUR = Active components/Total components× 100%.

The component is defined as the hardware to perform a specific logic function, such as AND, OR, NOT, and flip-flop. The active components mean the components that work for FM0 or Manchester encoding. The total components are the number of components in the entire hardware architecture no matter what encoding method is adopted. the total components are 7, including MUX−2 to indicate which coding method is activated. For FM0 encoding, the active components are 6, and its HUR is 85.71%. For Manchester encoding, the active components are 2, comprising XOR−2 and MUX−2, and its HUR is as low as 28.57%. On average, this hardware architecture has a poor HUR of 57.14%.

The transistor count of the hardware architecture without SOLS technique is 98, where 86 transistors are for FM0 encoding and 26 transistors are for

Manchester coding. On average, only 56 transistors can be reused, and this is consistent withits HUR.The coding-diversity

between the FM0 and Manchester codes seriously limit the potential to design a fully reusedVLSI architecture.

IV. VLSI ArchitectureDesign of FM0 Encoder and Manchester EncoderUsing SOLS Technique

The purpose of this sols technique to design a fully reused VLSI architecture for FM0 and Manchester encodings.the sols technique is separated into two parts: area-compact retiming and balance logic-operation sharing.. Finally, the performance evaluation of this technique is given.

I. Area-Compact Retiming

This method is mainly used in simplifying the FM0 encoder. For FM0 encoder, the state code of each state A(t) and B(t) is stored into separate flip flops. Since the transition of state code only depends on B(t), the encoder needs only a singlebit flip flop. Hence the block diagram is rearranged as shown in the diagram 7.

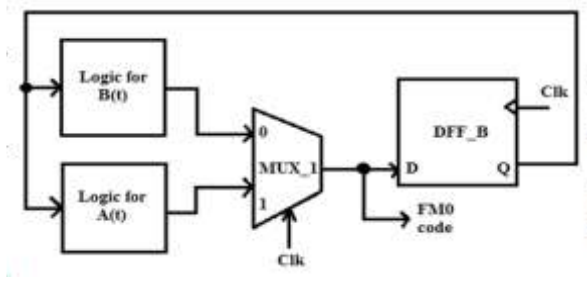


Fig 7: Simplified FM0 encoder

ii. Balance Logic Simplification

This technique deals with the Manchester encoder. Usually Manchester encoding can be treated as the XORing between the input signal and the clock. But it can also be treated as a Multiplexer where the clock is given as the select input and the data and its complement is given as the data input.It explain in below fig 8.

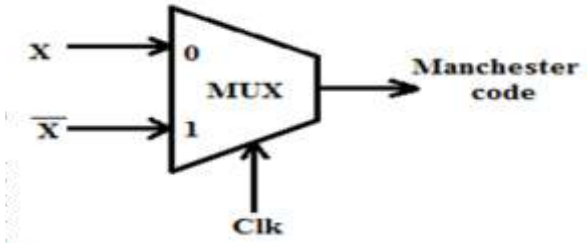


Fig 8.Simplified Manchester encoder

The above simplified encoders are combined together to form the SOLS encoder.This is shown in the diagram 9.

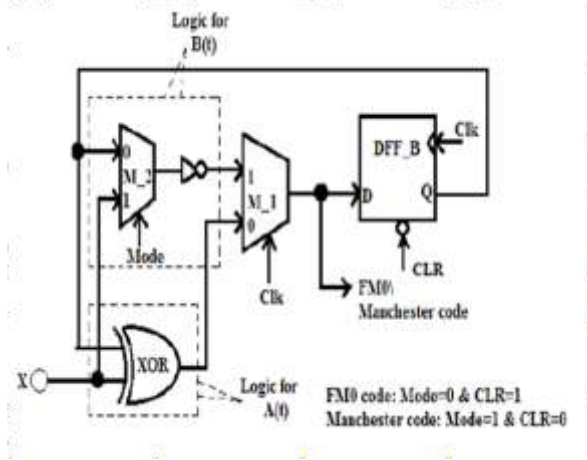


Fig. 9.SOLS encoder

The disadvantage of this SOLS encoder is that there is an unbalance in the computation time which results in glitch. In-order to avoid that, the NOT gate is moved to the output part of the first MUX and the XOR gate is replaced by the XNOR gate as shown in the diagram 10.

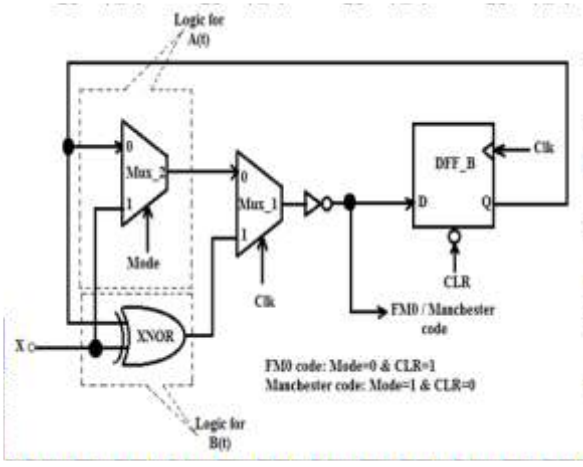
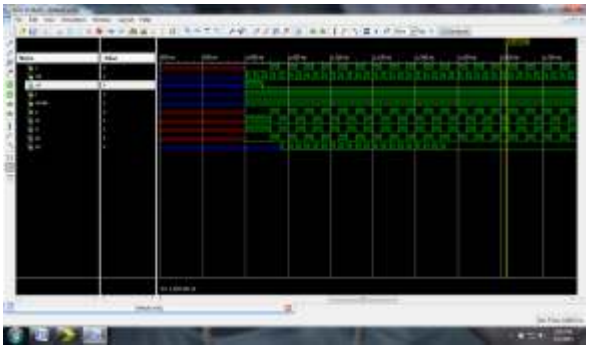


Fig. 10. Retimed SOLS encoder

Results

FMO Encoder



Manchester Encoder



SOLS Encoder



Conclusion

The highly transport system is applicable for smooth traffic control, vehicular safety etc. To implement such a system, DSRC communication protocol is used. In DSRC communication, the safety messages are encoded and transmitted to the other DSRC equipped vehicles which in turn enhances the security of the vehicles. The Manchester and FM0 Manchester encoding execute encoded data. But the wide range of code diversity limits the hardware utilization rate of such a reusable encoder. Hence, the new technology of designing such an encoder called SOLS technique. The SOLS encoder is of better advantage than the

Normal reusable encoder in terms of device
utilization. Besides the logic performance delay and memory usage of the system also get reduced.

REFERENCES

1. F. Ahmed-Zaid, F. Bai, S. Bai, C. Basnayake, B. Bellur, S. Brovold, etal., "Vehicle safety communications—Applications (VSC-A) final report," U.S. Dept. | 2. Trans., Nat. Highway Traffic Safety Admin., Washington, DC, USA, Rep. DOT HS 810 591, Sep. 2011. | J. B. Kenney, "Dedicated short-range communications (DSRC) standards in the United States," Proc. IEEE, vol. 99, no. 7, pp. 1162-1182, Jul. 2011. | 3. J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Herrtwich, "Design of 5.9 GHz DSRC-based vehicular safety communication," IEEE Wireless Commun. Mag., vol. 13, no. 5, pp. 36-43, Oct. 2006. | 4. P. Benabes, A. Gauthier, and J.Oksman, "A Manchester code generator running at 1 GHz," in Proc.IEEE, Int. Conf. Electron., Circuits Syst., vol. 3. Dec. 2003, pp. 1156-1159. | 5. A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis, "A 90nmManchester code generator with CMOS switches running at 2.4 GHz and 5 GHz," in Proc. 16th Int. Conf. Syst., Signals Image Process., Jun. 2009, pp. 1-4. +