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HIGH PERFORMANCE AND HIGH ENERGY-EFFICIENT PULSED LATCHES

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ABSTRACT

In the present era IC designers should design the circuits with less power dissipation without sacrificing the design performance. FLIP-FLOPS and latches are the devices which consume a large part of power. There is a need for energy efficient devices. This work is an attempt to improve the energy efficiency of latches in 65nm technology. In this paper a new category of pulsed latches are introduced. The topology is based on conditional pulse generation technique with push pull equipment. Two implementations of this idea are CP3L and CSP3L which are very fast when compared with TGPL.An improvement of 1.2x is achieved in ED product at the cost of increase in area which is less compared with the increase of area in overall system. Therefore these proposed latches are most suited for VLSI systems which require energy efficient devices.

KEYWORDS : Energy-efficiency,pulsed latches,VLSI,FLIP-FLOPS.

I. INTRODUCTION

FLIP-FLOPS and latches are the key devices in VLSI systems and micro processors in which they occupy a large part of the overall power. The clock network design is vital in VLSI systems. The energy consumption and speed of a device depends on clock network design. FLIP-FLOPS and latches consume approximately 80% of power of clock circuit and 30% of the total chip power [1]-[3].Latches and FLIP-FLOPS are extremely used in arithmetic pipelining. Clock frequency and overall throughput can be increased by breaking the combinational logic with the insertion of latches into the logic. As the demand for high energy efficient devices in VLSI systems growing each year, there is a need to design latches and FLIP-FLOPS which takes less power and work with high speed.

II. LITERATURE SURVEY

At present the energy consumption is becoming a problem in VLSI systems. Selecting a proper FLIP-FLOP technology and adapting a strategy to compare the performances existing topologies [4]-[8] is difficult. To estimate the performance of FLIP-FLOP or Latch, energy-delay (E-D) product can be very practical.

Out of those existing topologies only few topologies belong to pareto-optimal curve.Fig.1.shows the pareto-optimal curve. From the figure, only STFF[9] faster than Transmission gate flip-flop (TGFF)[10] for high speed targets. Adaptive coupling FLIP-FLOP (ACFF) is the recent device having energy saving of 77% at no data activity[11] and it is having larger delay when compared with TGFF.

Out of those topologies pulsed latches show best energy efficiency. From the Fig.1 TGPL shows minimum ED product. The schematic of TGPL is shown in Fig.2(a).

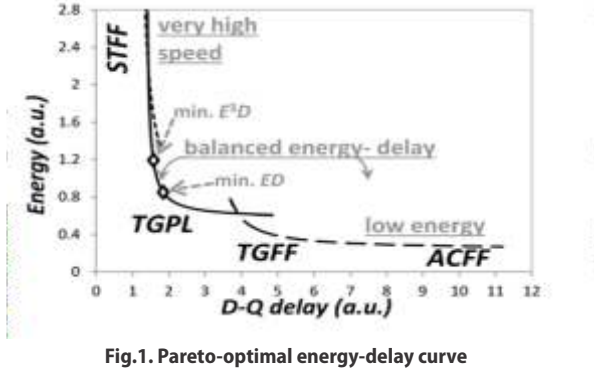


Fig.1. Pareto-optimal energy-delay curve

This technique uses a clock generator, which is shown in Fig.2(b).The clock signal is given as an input to both transmission gate and keeper circuit. Keeper circuit is placed before the output stage and it is used to stabilize the output.

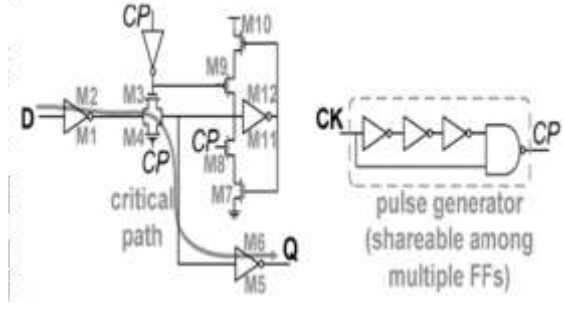


Fig.2.(a) TGPL architecture **b) Pulse generator**

The advantage of this method is low energy consumption. But placement of keeper circuit at the input node increases unwanted load at the input. The presence of transmission gate in the D-Q critical path increases parasitics. Due to these problems, there is a need for the evolution of high energy efficient devices [12],[13],[14].In this paper a new type of pulsed latches are introduced which improve ED product.

III.PROPOSED METHOD

The proposed pulsed latches topology in Fig.3 consists of a conditional pulse generator, which generates CPf and CPr signals. These are generated at falling clock edge and are used to drive half latches M1-M3, M4-M6 respectively, depending on the delayed signal QD. When compared with cascaded transmission gates, these are having less parasitics within the D-Q critical path. There are two paths which are driven by input D through M5 and M2.This gives the same load as traditional inverter stage as M1-M2 in TGPL.

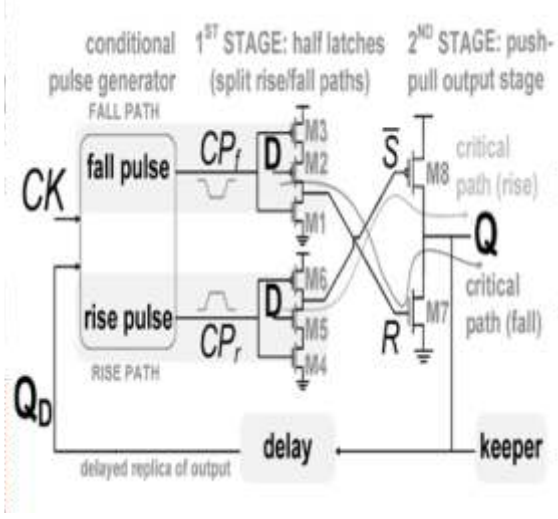


Fig.3. General topology of proposed technique

There is a push-pull stage M7-M8 which is an output stage. This technique reduces the driving circuit load by a factor of 2-3.This stage is driven by the signals R and Sbar. These signals resets and sets output Q respectively. The operation of conditional push pull pulsed latch is given by the waveforms depicted in Fig. 4 where at falling clock edge the pulse generator checks the previous value of QD. If QD= 1('0'), then the pulse CPf (CPr) is set to low(high).

If D=1(0), the half latch M1-M3(M4-M6) is disabled and R (Sbar)will be '0'('1').If D = 0(1), the latch M1-M3(M4-M6) is enabled and R(Sbar) is set to '1'('0') and the output Q will be'0'('1').

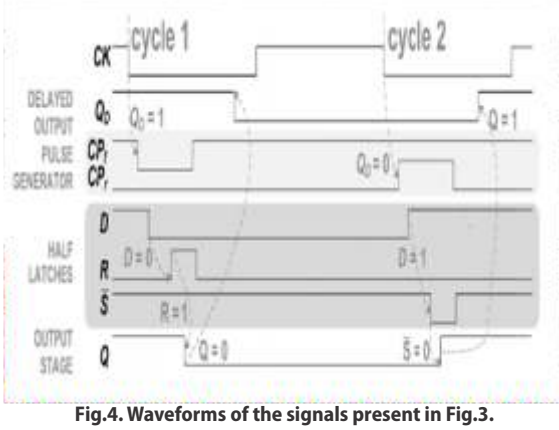


Fig.4. Waveforms of the signals present in Fig.3.

The output is maintained at the desired value by keeper circuit.The advantage of this configuration is moving the parasitics associated with the memory element to the output node which reduces the load to the input stage making the circuit as energy efficient and high performance device.

A.CONDITIONAL PUSH PULL PULSED LATCH (CP3L)

The diagram of CP3L technique in Fig.5 consists of a clock phase generator which is used to generate signals CK1, CK2, CK3 and CK4. The operation of clock generator is given in Fig.6.These signals are used to drive pseudo NAND and NOR gates. Generally CK1 and CK4 (CK and CK3) are complementary making either of the MOSFETs M18 or M19 (M20 or M21)on. But at the falling clock edge, signals CK1 and CK4 (CK and CK3) goes high(low) making both transistors off. Within the time period τinv–4τinv(0–3τinv) in Fig.6. the pseudo NAND(NOR) generates CPf(CPr) signal if QD = 1(0) or else CPf(CPr) will remains high(low).

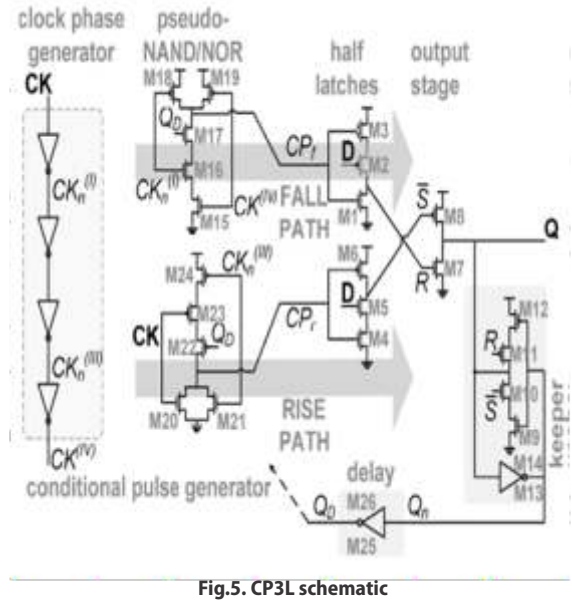


Fig.5. CP3L schematic

This produces alternative CPf and CPr signals which depends on previous output QD. This clock phase generator can be used as a shared one among multiple latches to reduce overhead. Then CPf and CPr signals will behave same as in general methodology and produces transitions in Q depends on D value.

There is a keeper circuit after output stage for the stability of output. At any time the half latch M1-M3 (M4-M6) has to drive only one transistor M11 (M10).That is only one transistor makes transitions. The operation of these latches is controlled by the width of CPf and CPr signals because only in this transparency window the input can affect the output. The delay of inverters in the clock generator controls the width of transparency window. There is a delay stage formed by two inverters M13-M14 and M25-M26 in the feedback loop which produces delayed signal QD.

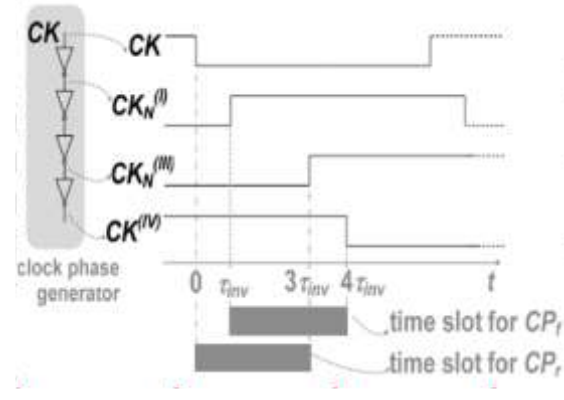


Fig.6. Waveforms of clock phase generator

The output Q can be directly connected as an input.This makes glitches in the output.These glitches are shown in Fig. 7.During the same input stage if Q makes transition to zero then CPr high signal is generated. But it does not affect operation,

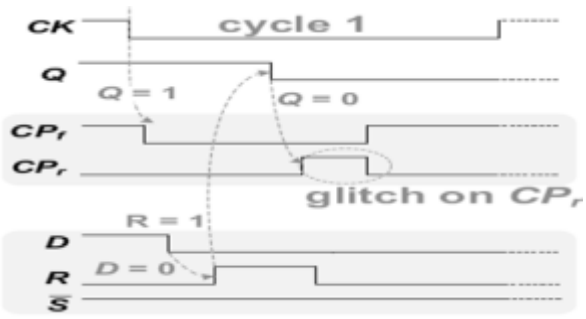


Fig.7. Glitch in CPr without delay stage

because D is having the value of zero at this stage. So M5 transistor is off and it does not reach the output. Even when D=0 the transistor M5 is on and sets Sbar to zero and it sets the Q to desired value '1'.In this way glitches can be avoided using delay stages in the feedback paths.

B.CONDITIONAL SHAREABLE PUSH-PULL PULSED LATCH(CSP3L)

In CP3L the pulse generator cannot be shared. But implementing conditional logic in to the technique pulse generator can be shared. The resulting technique is CSP3L.The schematic of CSP3L topology is given in Fig.8(b).

In CSP3L static NAND and NOR gates are used with clock phase generator as shareable pulse generator as shown in Fig. 8(a) gives CPf,ext and CPr,ext signals. These signals can be shared among latches which behave similarly as CPf and CPr signals. These external pulses are enabled by the switches formed by the transistors M15-M22.

The topology consists of two transmission gates and two keeper circuits where they do the same operation as in CP3L.In order to provide two control signals to transmission gates, there are two inverters in the delay stage. The area of CSP3L is approximately same as CP3L because of equal transistor count.

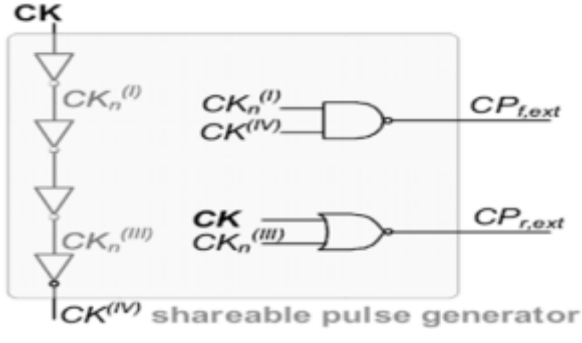


Fig.8(a). Shareable pulse generator

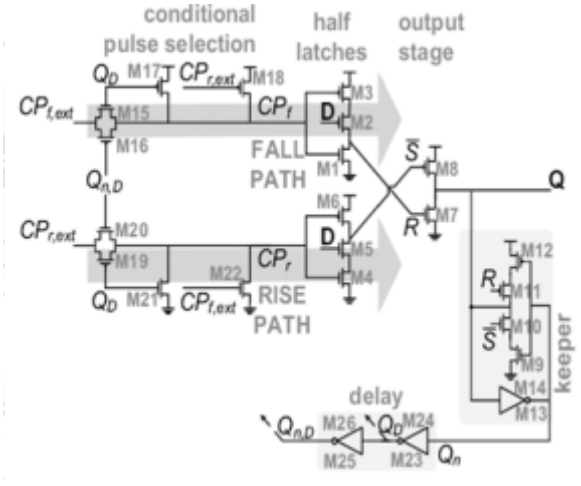


Fig.8(b). CSP3L schematic

The operation of CSP3L is same as CP3L, except the inclusion of shareable logic. Depending on the value of QD the signals CPf,ext and CPr,ext are transmitted to half latches.Then the behavior of CSP3L is same as CP3L and produces resultant outputs.

IV.MEASUREMENT RESULTS

The operation of CP3L and CSP3L is tested in LTSPICE tool. The simulated waveforms of CP3L and CSP3L are given in figures Fig.9(a), Fig.9(b) respectively.

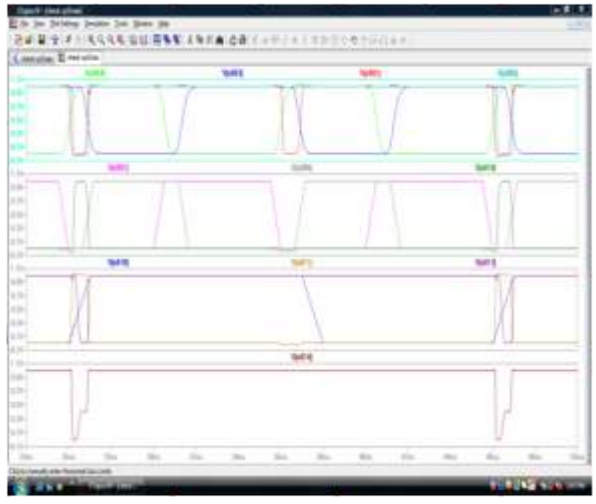


Fig.9(a). Waveforms of internal signals of CP3L.

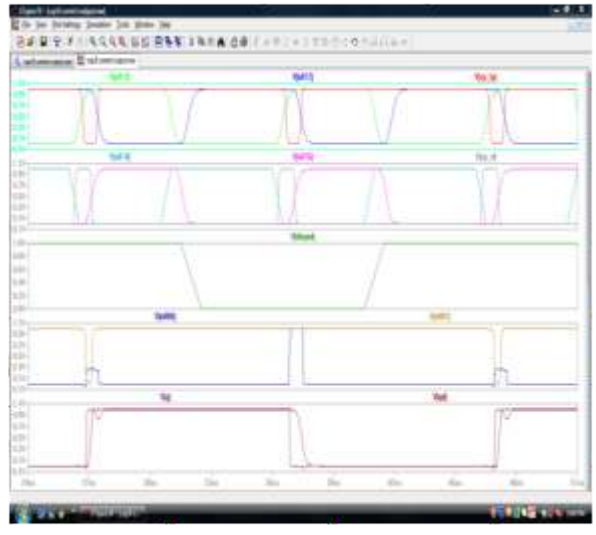


Fig.9(b). Waveforms of CSP3L internal signals

Layout parasitics can be used to optimize transistor sizes [15].There is 1.9X increase in area of CP3L and CSP3L when compared to TGPL.The layouts of TGPL,CP3L,CSP3L are given in figures Fig.10(a),Fig.10(b),Fig.10(c) respectively.

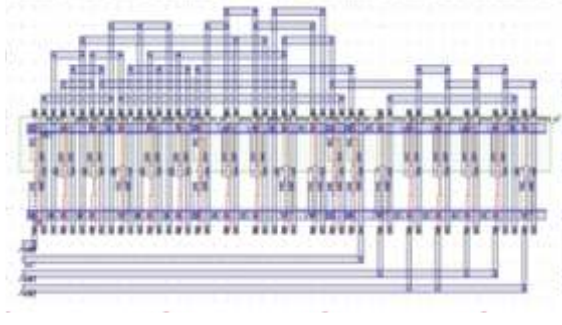


Fig.10(a). Layout of TGPL

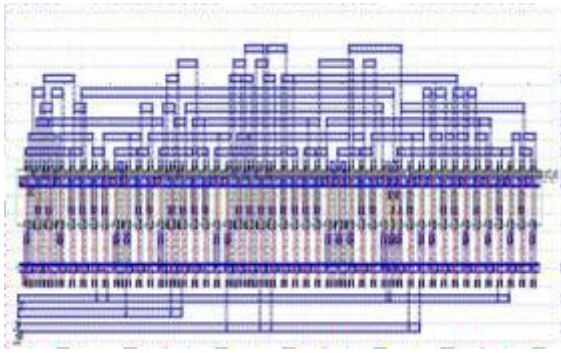


Fig.10(b). CP3L Layout

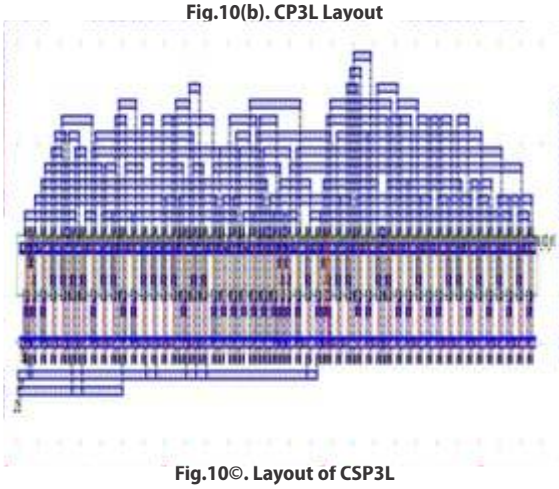


Fig.10©. Layout of CSP3L

The energy delay tradeoff of the proposed methods in Fig.11 shows that the minimum ED of CP3L and CSP3L is 1.2X better than TGPL.

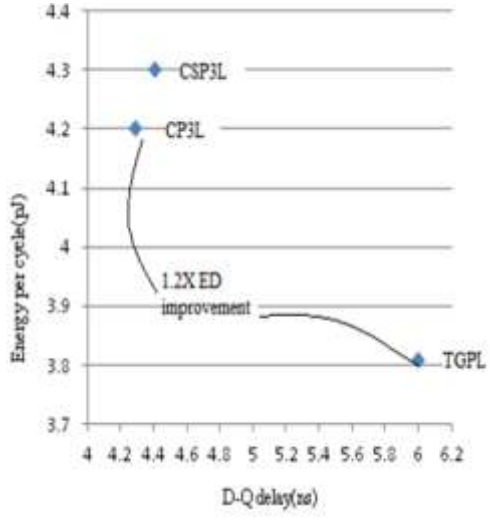


Fig.11. Energy-Delay Tradeoff

V.CONCLUSION

This paper proposes the design which has split paths and push pull stage that reduces the D-Q delay.There is a 1.35x improvement in speed when compared to TGPL.The energy delay product of proposed latches is improved by a factor of 1.2.There is 1.9x increase in area than the smallest existing latch TGPL but it is lesser compared to overall increase in chip area. The energy and performance of CP3L and CSP3L are approximately equivalent. Therefore they are equally important for high energy efficient devices.

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