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IMPLEMENTATION OF HIGH SPEED 8-BIT VEDIC MULTIPLIER USING BARREL SHIFTER BY EMPLOYING CPLDS

CH. Sandhya Rani Department of Electronics and Communication Engineering Narayana Engineering College,Nellore-524003, A.P, India

M. Muralidhar Department of Electronics and Communication Engineering Narayana Engineering College,Nellore-524003, A.P, India

ABSTRACT

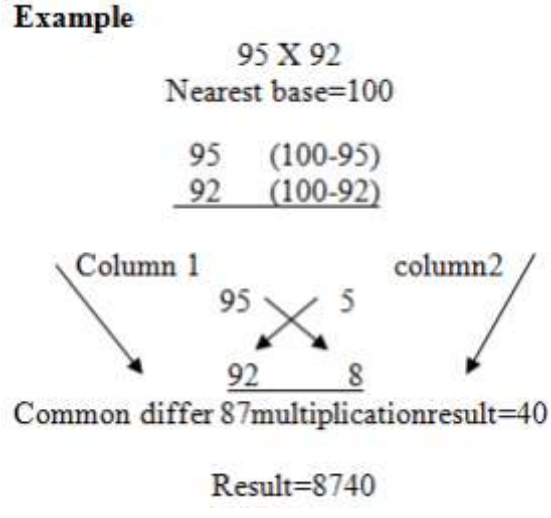
This work introduces a methodology that exploits Vedic multiplier scheme and reduces multiplier complexity by using barrel shifters rather than generating product terms and combing them typically done in array multipliers. The multiplier and multiplicand are represented in base plus offset forms. The base of the given number is directly the 2^n such that 'n' is the position of the most significant '1' in the given number. The offset are the residue values to the boundaries followed by 2^n.where 'n' is the length of the word, limiting to 16 bit. This method is best suitable for numbers that have a small offset relative to a large higher order base index, so that the offset multiplication could be performed using a lower order array multiplier saving the area. Popular CPLD devices assumed for the implementation of the design rather than FPGAs in order to count number of gates that would be used. This directly gives the reduction factor with respect to area compare to a full fledged multiplier. The same is found to be around 12.5% overall improvement in area, to implement the design rather than FPGAs for area reduction at the gate level. By employing CPLDs there will be around 12.5% area reduction for VLSI applications.

KEYWORDS : Barrel shifters, adders, Vedic multiplier, base-offset resolvers.

I. INTRODUCTION

This paper mainly focussed on the optimization of area by reducing the number of combinational gates. This optimization can be done by employing the formulae called "Nikhilam sutra", a Vedic mathematic formulae for the simplification of multiplication. Here we employed the sutra called modified "NIkhilam sutra" using barrel shifters. Nikhilam sutra means 'all from 9 and last from 10'. Evnthough

"NIkhilam sutra" is applicable to all cases of multiplication; it is more capable when the numbers involved are massive. Nikhilam sutra introduces the concept of equating the bases to the nearest powers of 10, 100, 1000 etc. We first illustrate this sutra by multiplication of two decimal numbers (95 * 92) where we choose the base as 100 which were nearest to and greater than both these numbers.



Multiplication by using Nikhilam Sutra

The right hand side (RHS) of the product term can be obtained by multiplying the numbers of the column 2(5 *8=40). In the same way the left hand side (LHS) of the product term can be attained by cross subtracting the succeeding number of column2 from the initial number of column 1 or vice versa, that is, 95-8=87 or 92-5=87. The finishing result can be attain by simply concatenating RHS and LHS (Answer=8740).

The mathematical expression for the modified "Nikhilam sutra" is given below.

Result = (X1+O1)*(X2+O2)
=(X1*X2)+(X1*O2)+(X2*O1)+(O1*O[1]

Where
X1=base with index K2.
X2=base with index K2.
O1=offset value1for an 8 bit number
O2=offset value2 for an 8 bit number.

The term (X1*X2) performs the multiplication operation for the multiplier and multiplicand.

(X1*O2) and (X2*O1) are the 8-bit barrel shifters. The barrel shifter performs the simple shifting operations rather than multiplying the two numbers.

(O1*O2) performs the full fledged multiplication that uses only 8-bit multiplier and multiplicand. That means rather than multiplying all the values, only the smaller offset values are get multiplied.

II. LITERATUTE SURVEY

In this paper, authors employ a nikhilam sutra, for implementing this sutra they use the multiplier architecture which contain the top level Module(Figure1) & overall block diagram Module(Figure2) which are the fundamental parts of this project. In this work we have put into achieve a high speed Vedic multiplier by using barrel shifter. We have used 8-bit barrel shifter which requires only single clock cycle for 'n' number of shifts, or counts [1]. This paper was proposes implementation of a high data rate adder on Field Programmable Gate Arrays (FPGA). Digital Signal processing applications are categorized by the data rate or the throughput of the system[2].A standard processor central processing unit uses an ample amount of processing time in performing arithmetic operations, primarily multiplication operations. Multiplication operation is one of the vital arithmetic operations and it requires significantly more hardware resources and processing time other than addition and subtraction.In this paper, comparative of different multipliers are prepared for low power constraint and high speed [3]. This paper gives information about "Urdhva Tiryakbhyam" algorithm of earliest indian Vedic Mathematics which is

used for multiplication of two or more operands for getting better speed, area parameters of multipliers. Vedic Mathematics has been suggests one more formula for multiplication of large numbers that is modified "Nikhilam Sutra" which can also boost the speed of multiplier by reducing the number of iterations or counts [4].

Udhrva sutra performs faster than for small inputs and nikhilam sutra for larger inputs. Here a novel integrated Vedic multiplier is proposed [5].

III. PROPOSED MULTIPLIER ARCHITECTURE DESIGN

The proposed multiplier architecture is employed with two block diagrams. The hardware description of the proposed multiplier is partitioned into two blocks [6]. They are as follows.

1. Top-level diagram
2. Detailed block diagram

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1. Top-level diagram

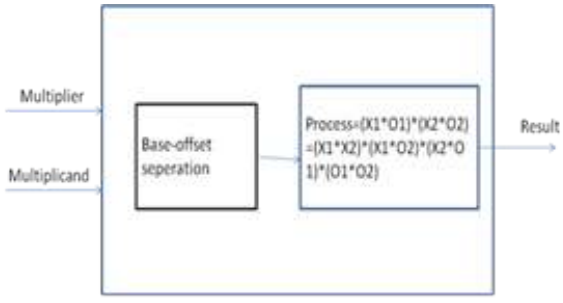


Figure1. Top-level diagram

Operation The multiplier and multiplicand are represented in base-offset forms. The base of the number can be obtained by equating the corresponding MSB bit to'1' and the remaining bits to zeros. The offset value can be obtained by subtracting base value from the input what we are giving [7]. Then the actual process of multiplication of bases and offset values can be done. Here we are taking both multiplicand and multiplier as 16 bits and the result we got is 32 bit. The result can be obtained by simply concatenating the multiplicand with the multiplier.

The simple formulas for the base and offset values are as follows.
Base=2^L-1, where 'L' is the location of the bases with indexes K1, K2.
Offset=data input-base [8].

2. Detailed block diagram

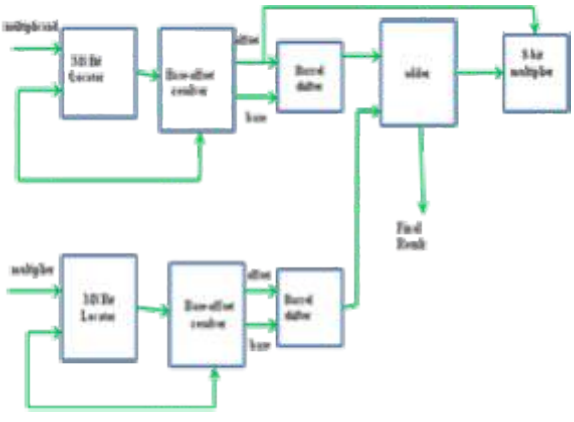


Figure2.Detailed block diagram

Operation The above block diagram is partitioned into two Ms-bit locators, two base-offset resolvers, and two barrel shifters. The base-offset separation can be done by using the process block following th equation [1]. Base is nothing but finding the MSB bit '1'position.That means the base can be obtained from the MSB bit locator. Now the process of base-offset separation can be done by using the base-offset resolver. From the base-offset resolver we get the respective base-offset values. The bas is 16-bit length, where as the offset is 8-bit length[9].

The outputs of the base-offset resolver are given to the barrel shifter. In barrel shifter shifting operations can be done rather than multiplying the two big numbers. In this we require two 8-bit barrel shifters which may require single clock cycle for 'n' number of shifts. The barrel shifter used at different levels of design may drastically reduces the time and lessen the effort, when compared to the conventional multipliers like array multipliers[10].

In this proposed work we used the vedic multiplier using barrel shifters. This paper employs modified "Nikhilam sutra" due to its feature of reducing the number of partial products. Whenever, the product terms are reduced by asset of this the speed increases, and also the performance of the multiplier is also improves. The final result can be obtained from the adder circuit which may the concatenation of multiplier and multiplicand. Here we use 16-bit multiplicand and 16-bit multiplier and the result is 32-bit.

IV.SIMULATION RESULTS

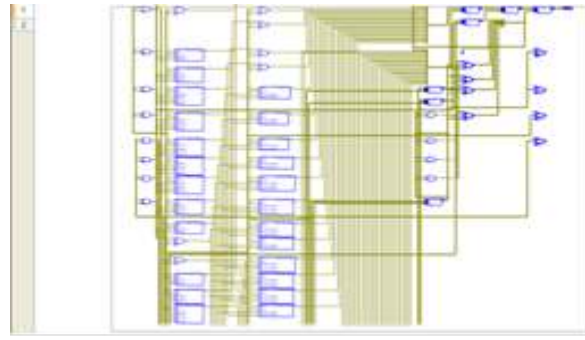


Figure3. RTL Schematic 1

This RTL schematic was generated from the Xilinx 9.1 ISE simulator. Extension for this can be represented in below.

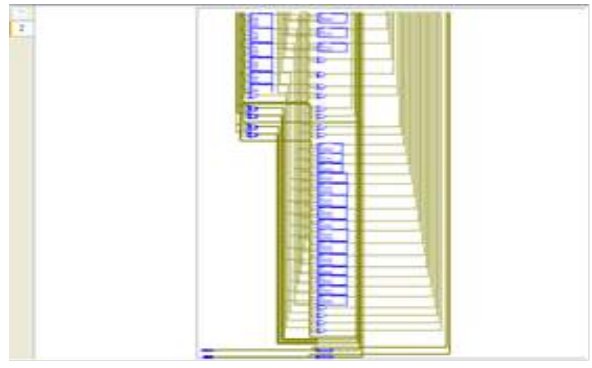


Figure 4.RTL schematic 2

This schematic was generating using Xilinx 9.1ise simulator.

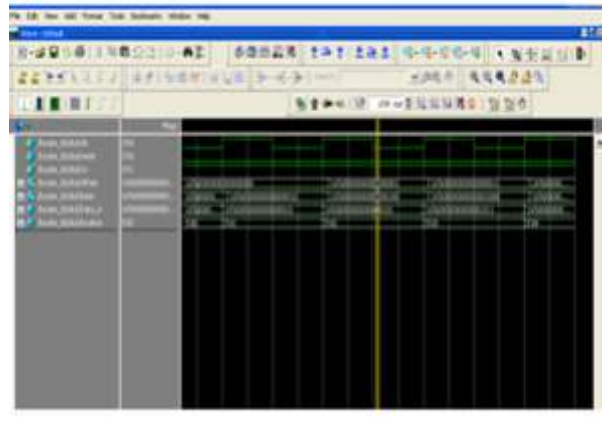


Figure5. Simulation result for top-module

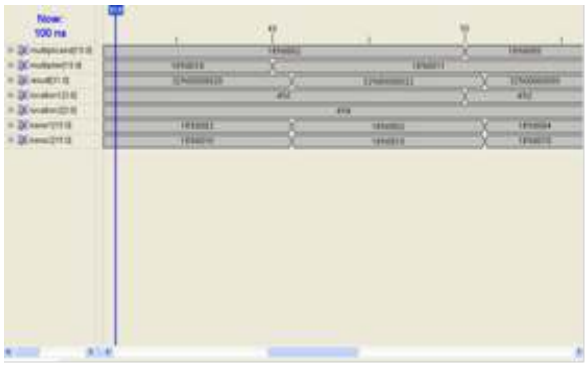


Figure6. Simulation Result for final block diagram

The simulation results for top-module and final block diagram are generated from the Xilinx 9.1ise simulator by using Figure1 and Figure2.

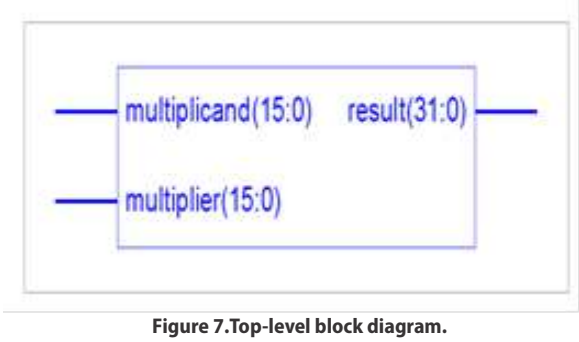


Figure 7.Top-level block diagram.

This top-level block diagram can be obtained from the Figure 1.

V. COMPARISION OF CHIP AREA BY EMPLOYING CPLDS

Gates used	Gate count when direct 16-bit multiplier is used	Gates used	Gate count when modified Nikhilam Sutra is used	%of reduction
				In gate count
And2	721	And2	532	18.90%
Or2	446	Or2	312	13.40%
Xor2	464	Xor2	242	22.20%
Total	1632	Total	1428	12.50%

We know that by employing CPLDs the overall area can be reduced at the gate level. There will be almost 12.5% reduction in area can be observed by employing CPLDs in application to the VLSI.

VI. CONCLUSION

This work mainly aimed to reduce the chip area by employing XC 9500 CPLDS.There by employing these CPLDS we got around 12.5% reduction in chip area by employing our proposed modified Nikhilam sutra rather than CPLD direct 16-bit multiplier. By optimizing the offset values to the smaller values the area gets lesser so that we can get the optimized result.The future scope of this project involves further more optimization of chip area at the gate level.

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