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# Testing of Mixed Signal Ics: A Review

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**ABSTRACT**

*This paper basically gives a review on various testing techniques adopted for the detection of faults in a Mixed signal IC. Charge Pump Phase locked loop i.e. CP-PLL is considered here as mixed signal IC for reviewing all the testing methods adopted over the years. Design for testability, DFT must be a centre element for the design process these days. With circuit complexity increasing and component size decreasing, the testability of electronic circuits are more crucial as testing is becoming even more demanding. This rising popularity increases the demand of preparing the low cost testing circuitry. Because of the tight feedback CP-PLL is one of the difficult electronic circuit to which testing strategy is to be adopted. Here in this paper all the methods are reviewed and a comparison chart is shown having the details of area overhead and efficiency.*

**KEYWORDS : CP-PLL, DFT, area overhead, mixed signal IC.**

## INTRODUCTION

With the invention of transistor electronics industry has experienced huge revolution in all the aspects, especially in the field of integration technology. As Very Large Scale Integration, VLSI industry has been growing rapidly, testing techniques are require having considered the impact on time to market as well as the production cost of electronic industry. Mixed signal IC which incorporates both the analog and digital sub circuits on the same chip are very popular now a days. And hence testing of such ICs are also becoming crucial for above stated reasons (C. S. Taillefer, G. W. Roberts and L. Balado et al. 2005, 2006).

However such ICs are not easier to test, because not only the demand for testing increases, but also the challenge for testing both the domains at the same time leads to the problem for testing environment, time consumption and the resources used. With integration technology advancing day by day number of component available in a die area has increased amusingly. Hence testing is not easy with the added difficulty of mixed signal ICs. The analog testing schemes are yet to be advanced because they still rely on the measurement of catastrophic faults only, though the recent researches in this field shows better results. But not up to the mark.

However the state of are in case of digital systems are advanced enough and applied successfully too. CP-PLL is the mixed signal block used in large applications such as clock distribution, phase demodulation, time recovery etc. hence it is important in application of the wireless phones, optical fiber links, and microcomputers.

Various testing techniques used for the testing of CP-PLL are described here in brief. Before that let me introduce the CP-PLL first.

### What is CP-PLL?

A PLL is a feedback control loop circuit that synchronizes an output signal (generated by an oscillator) with a reference or input signal in both frequency and phase. Figure 1 shows the block diagram of the classical CP-PLL (C. L. Hsu, Y. Lai, S. W. Wang and Hsu et al. 2005, 2009), which consists of phase/frequency detector (PFD); charge-pump circuit, which transforms the digital Up; down signals into analog voltages; and loop filter, which attenuates the high frequency components from the analog voltage generated by the charge pump circuit; VCO, which generates a clock, with the frequency of the clock being controlled by control voltage V generated by the loop filter.

The PFD compares the output signal output clock generated by the VCO with reference-clock. Figure 2 conceptually demonstrates the operation of a PFD for two cases: (a) the two input signals have the same frequency, and (b) one input has higher frequency than another input.

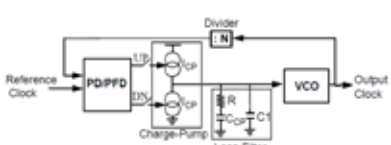


**Figure 1: A classical CP-PLL.**

Notably the up and down signal are used to increase and decrease the frequency of the PLL_out signal of the VCO. Then, the combination of the charge-pump circuit and the loop filter converts these digital signals into an analog control voltage for the VCO. A simple second-order, low pass filter composed of a resistor and two capacitors is considered to filter the signals coming from the charge pump. Finally, the VCO delivers output signal whose frequency is proportional to the analog control voltage applied at its input.

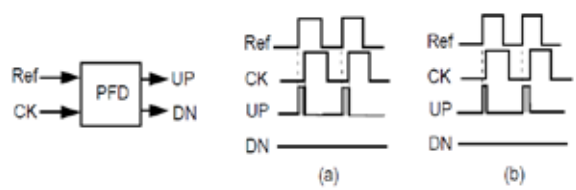


**Figure 2: Operation of a PFD: (a) fref=fCK, and (b) fref>fCK**

Figure 3 shows Catastrophic fault model which always has a strong impact on the DFT circuits, because the measurement of the faults and the total fault coverage will be decided on different fault models (Hsu et al. 2005). In other words, the catastrophic faults in the charge pump, loop filter, and VCO are identified as follows (Hsu et al. 2005): gate-to-source short; gate-to-drain short; drain-to-source short; Resistor short; Capacitance short; Gate open (GO); Drain open; Source open; Resistor opens (RO). In the fault simulation, a low resistance (1 Ω) and a high resistance (10 MΩ) are frequently used to model a short fault and an open fault, respectively.

**By Karim and Bozena :** Starting with the first research work shown over here by the authors Karim and Bozena , tried to implement the mixed signal testing architecture based on the vector-less dynamic test strategy, which actually partition the circuit under test in to the different parts so that testing of that circuitry becomes easier. The test has been evaluated for some typical analog and mixed signal blocks, but practical implementation of the BIST structure was missing there. Figure 4 shows the architecture (Karim and Bozena, 1996):

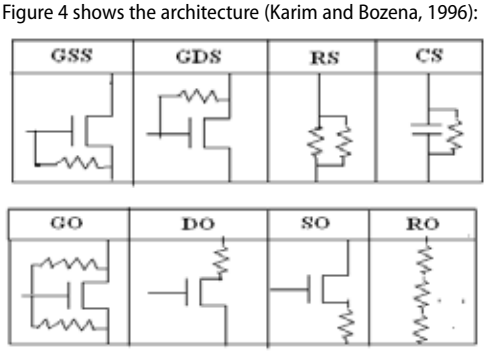


**Figure 3: Catastrophic fault models**

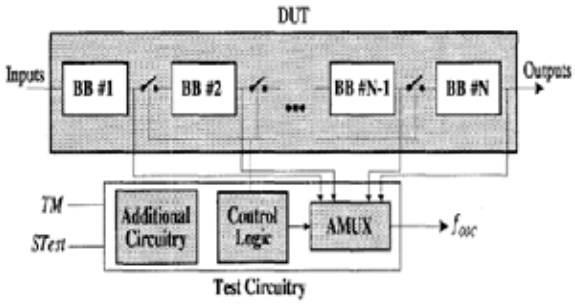


**Figure 4: Simplified test structure of the oscillation test strategy by Karim and Bozena**

**By Prashant giri, Mani soma, and devaravanadurg :**The second research work shown is given by the authors Mani Soma , Giri and devarayanadurg. That technique is actually based on the boundary scan architecture and designed for the PLL. They converted the close loop PLL system to the open loop system so that verification of the different parameters becomes easy. But the area over head due the insertion of the lock measurement adjustment techniques increased in this case of about 10%. Figure 5 shows the architecture (Prashant et al. 1997).

**By KIM and Soma:** The testing architecture shown in Figure 6 has been given by the authors KIM and Soma which has following drawbacks: First the phase detector in the PLL cannot be tested for defects with the existing CF-BIST structure. This is due to the fact that the 4-by-2 multiplexer is right after the phase-detector, thus the test signals from the controller do not go though the phase-detector.

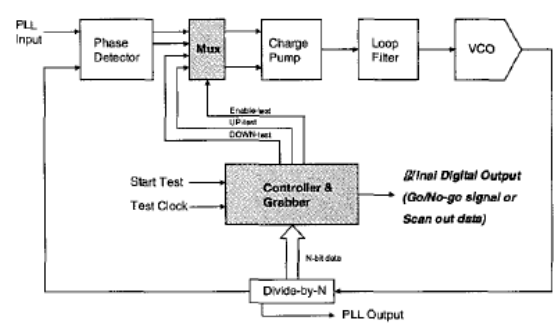


**Figure 5: Testing architecture given by the giri and soma**

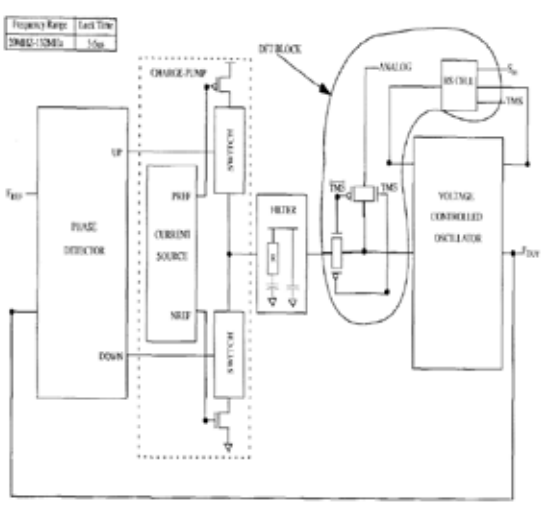

**Figure 6: BIST architecture given by the Soma and KIM.**

And second drawback in using the multiplexer after the phase-detector is the introduction of delay in the tight feedback loop. This can be solved by incorporating the multiplexer function at the output of the phase-detector in the PLL design stage. Figure 6 shows the architecture (Kim and Soma, 2001).

**By Jayabalan, Leong, Sang, Iyer, and Tay:** The method adopted in this paper results in either excessive or insufficient testing of the circuit and requires dedicated testing and long testing time. Figure 7 shows the architecture (Jayabalan et al. 2003).

**By F. Azais, Y. Bertrand, M. Renovell Ivanov and S.Tabatabaei**

The method adopted in this paper is dividing and conquer approach by partitioning the circuit, and applying specific test to each block. The technique devised simple digital testes for each block however this approach has a loading problem for a sensitive analog node. Figure 8 shows the architecture (F.Azais et al., 2003)

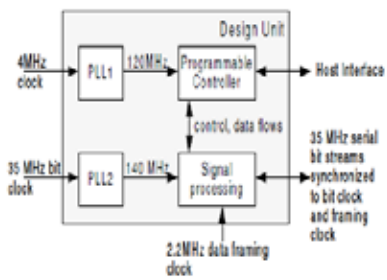


**Figure 7: Test architecture given by the Jayabalan, Leong, Sang**

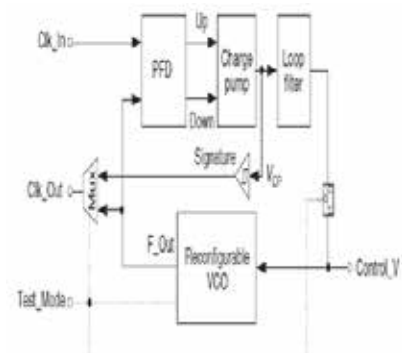


**Figure 8: Test architecture given by F.Azais, Y. Bertarand, M. Renovell Ivanov and S.Tagatagaei.**

**By J Han , D Song and S Kang**: A structure test, which used the change in phase difference generated by selectively alternating the feedback frequency , is presented, This approach is basically applies the test input stimulus to every block, a great number of circuits are added to the feedback loop path, the delay characteristic is the constraint on a BIST PLL design. Figure 9 shows the architecture (J.Han et al.2004).

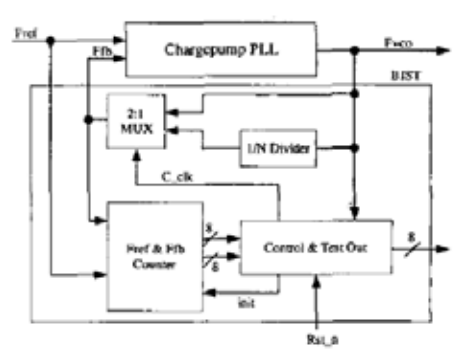


**Figure 9: All digital Test architecture given by the J Han, D Song, S Kang.**

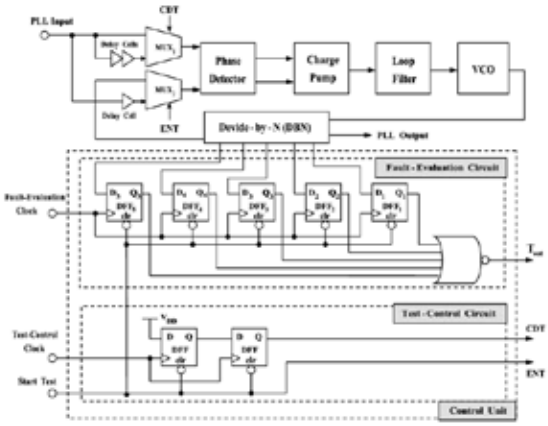


**Figure 10: BIST architecture given by the Hsu, Lai and Wang.**

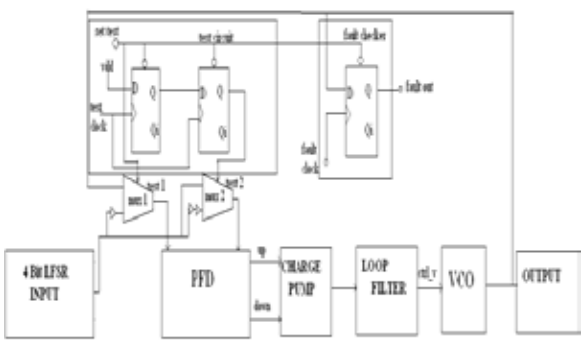


**Figure 11: DFT architecture given by the Ashish and Anil.**

**By Hsu, Lai and Wang**: A defect oriented test technique, which controlled the charge and discharge operation of the charge pump and loop filter for testing & did not alter any existing analog circuit of the PLL; thus the loading problem in analog node can be solved. . Figure 10 shows the architecture (Hsu et al. 2005).

**By Ashish and Anil**: Structure adopted by Hsu, Lai and Wang have been simplified and modified in proposed approach to give more efficiency to digital testing for a classical CP-PLL circuit. Possible faults in any block of the CP-PLL can be detected using the proposed CP-PLL DFT structure. The proposed structure has the following advantages:-

The technique did not alter any existing analog circuit of the PLL; because it is applied at the digital part i.e. PFD and controlled by that only. Thus the loading problem for an analog node can be solved. More over the proposed structure utilizes the existing blocks of CP-PLL i.e. charge pump and loop filter as stimulus generator and VCO as measuring device which ultimately reduces the area overhead and increases the efficiency of proposed structure. Figure 11 shows the architecture ( Ashish and Anil, 2012).

All the architectures used for testing the mixed signal ICs have been discussed above. Table 1 shows the details in brief with the names of all the authors and their research work. Remark has also been included showing the characteristics, advantages and area of improvement. Table 2 shows the comparison between all the methods discussed in this paper (Ashish and Anil, 2012). Area overhead and the efficiency are two important measures for testing the mixed signal IC. Table clearly shows that method adopted by authors Ashish and Anil has better efficiency and less area overhead

**TABLE – 1**
**BRIEF ABOUT RESEARCH WORKS DONE FOR PLL TESTING**

| S N | Author | Year | Remarks |
|---|---|---|---|
| 1. | Ashish Tiwari And Anil Kumar Sahu | 2012 IEEE (ncccs) | The method described by authors Hsu et al. in their paper have been simplified and modified in proposed approach to give more efficiency to digital testing for a classical CP-PLL circuit. Possible faults in any block of the CP-PLL can be detected using the proposed CP-PLL DFT structure. |
| 2. | C. L. Hsu Y. Lai S. W. Wang | 2008 IEEE | A defect oriented test technique, which controlled the charge and discharge operation of the charge pump and loop filter for testing & did not alter any existing analog circuit of the PLL; thus the loading problem in analog node can be solved. |
| 3. | J. Han D. Song S. Kang | 2005 IEEE | A structure test, which used the change in phase difference generated by selectively alternating the feedback frequency , is presented, This approach is basically applies the test input stimulus to every block, a great number of circuits are added to the feedback loop path, the delay characteristic is the constraint on a BIST PLL design. |
| 4. | F. Azais Y. Bertrand M. Renovell Ivanov S.Tabatabaei | 2004 IEEE | The method adopted in this paper is dividing and conquer approach by partitioning the circuit, and applying specific test to each block. The technique devised simple digital testes for each block however this approach has a loading problem for a sensitive analog node. |
| 5. | J. Jayabalan et al | 2003 IEEE | The method adopted in this paper results in either excessive or insufficient testing of the circuit and requires dedicated testing and long testing time. |
| 6. | Seongwon Kim, Mani Soma | 2001 IEEE | The phase-detector in the PLL cannot be tested for defects with the existing CF-BIST structure. This is due to the fact that the 4-by-2 multiplexer is right after the phase-detector, thus the test signals from the controller do not go though the phase-detector. Another drawback in using the multiplexer after the phase-detector is the introduction of delay in the tight feedback loop. This can be solved by incorporating the multiplexer function at the output |
| 7. | Prashant Goteti Giri Devarayanadurg Mani Soma | 1997 IEEE | PLL in a system incorporating IEEE 1149.1 boundary scan architecture. This strategy, which in essence converts a feedback system into an open loop system, allows the convenient verification of the frequency operating range of the PLL while in test mode. But constitutes in area overhead of about 10% for DFT. |
| 8. | Karim ARAB1 and Bozena KAMINSKA | 1996 IEEE | A new vector-less dynamic test strategy based on Converting the CUT to a circuit which is easier to test has been proposed and evaluated for some typical analog and mixed-signal building blocks. But they have not implemented the practical BIST solution for mixed-signal circuits. |

**TABLE – 2**
**COMAPRISON BETWEEN PLL TESTING TECHNIQUES**

| Parameter | Ashish & Anil 2012, IEEE NCCCS | Hsu, Lai and Wang 2008, IEEE | Han, Song and Kang 2005, IEEE | Azais et al 2004, IEEE |
|---|---|---|---|---|
| Testing type | Defect oriented test | Defect oriented test | Defect oriented test | Defect oriented test |
| Loading problem | Solved | Solved | Solved | Not |
| Loop typ | Broken | Broken | Broken | Broken |
| Test Accessibility | Simple | Simple | Simple | Simple |
| Covered block | All | All | All | Partial |
| Test time | Extream Fast | Very Fast | Fast | Fast |
| Area overhead | 3.025% | 4.48% | 2.78% | Low |
| Fault coverage | 98.2% | 97.9% | 97.2% | 88.2% |

## CONCLUSIONS

In conclusion we can say that Design for testability architecture is the best technique for testing of Very large integrated ICs. Over the years various methods have been adopted as discussed in this paper but it is proved from the outcome of recent works that Design for Testability architecture is best among them because of two most important reasons i.e. area overhead and the fault coverage. Area overhead is nothing but the measure of extra area consumed for the incorporation of testing circuitry. It is essential and also required that it has to be as minimum as possible without disturbing the original characteristics of the IC to be tested, so that power dissipation can be reduced. Cost is also one of the major concerns for the production of Mixed Signal IC, with increasing fault coverage and decreasing area overhead we can manage with this issue too.

On observing table number 2 it can be clearly said that the work suggested by the authors Ashish Tiwari and Anil Kumar Sahu provides the best fault coverage over the considerable area overhead. Though the loop of PLL is broken to include the testing circuitry but it is done on the digital part which is less sensitive to noise and loading effect as compare to the analog sub circuit. However the jitter measurement is the major area of concern in the computational fault testing, because it yields the data loss in communication system or computation errors in high speed computation systems, which is lacking. Restated that the proposed architecture gives the computational simulations result only which has to be verified by actual chip implementation. Overall the proposed structure provides the cost effective solution to the engineers to test entire CP-PLL.

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