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Fpga Implementation of Direct Digital Frequency Synthesizer with Cordic Algorithm

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ABSTRACT

The modern communication systems and software radio based applications demands fully digital receivers, consisting of only an antenna and a fully programmable circuit with digitalmodulators and demodulators. A basic communication system's transmitter modulates the amplitude,phase or frequency proportional to the signal being transmitted. An efficient solution (that doesn'trequire large tables/memory) for realizing universal modulator is CORDIC (CO-ordinate RotationDigital Computer) algorithm. The CORDIC algorithm is used in the rotation mode, to convert thecoordinates from polar mode to rectangular mode. The radius vector(r) and angle (θ) of a CORDICprocessor can be programmed to generate the ASK, PSK and FSK signals. Modelsim simulator toolfrom mentor graphics will be used for functional simulation and verification of the modulator. TheXilinx synthesis Tools (XST) will be used to synthesize the complete modulator on Xilinx Spartan 3Efamily FPGA (XC3S500E). Xilinx placement & routing tools will be used for backed, designoptimization and I/O routing.

KEYWORDS : CORDIC Algorithm, CORDICArchitectures, DDS, Communication System.

1. INTRODUCTION

Coordinate rotation digital computer (CORDIC) is a special purpose computer tocompute many transcendental and nonlinear functionns. This was proposed byVolder in 1959 [1]. The functions that can be computed using a CORDIC computerinclude logarithmic, trigonometric, hyperbolic, etc. [2]. CORDIC hasbecome a popular tool to implement several digital systems, especially in the areasof digital signal processing (DSP), communications, computer graphics, etc. Thesimplicity of CORDIC lies in the fact that it can compute any of the abovementionedoperations using shifts and additions. The operating mode and thecoordinate system are two key factors to compute the desired functions in theCORDIC. Many signal processing and communication systems operate CORDICin circular coordinate system.

Frequency synthesizers, sometimes also called oscillators, are essential units ofmanycommunication systems. Many communication systems employ digitalsubsystems in their units, thus making the usage of digital systems more ubiquitous.Direct digital synthesizers (DDS) are a class of frequency synthesizers indigital domain, which generate waveforms of desired frequencies [3]. Thesegenerate waveforms like sine, cosine, triangular, square or rectangular, saw tooth,etc. As mentioned earlier, these have wide applications in satellite communicationsystems, RF signal processing, etc. DDS offers many advantages over analogoscillators such as precise tuning resolution of output frequency, fast hopping ofphase that reduces phase related errors, and many more.Section 2 discusses the background, Sect. 3 discusses the proposed design,Sect. 4 discusses the implementation and results, and Sect. 5 concludes the paper.

2.BACKGROUND

DDS or direct digital frequency synthesizer (DDFS) consists of the following

blocks: phase accumulator (PA), phase-to-amplitude converter (PAC), digital-toanalogconverter (DAC), and a low-pass filter. The block diagram of the system isshown in Fig. 1.The PA accumulates the phase according to the frequency control word (FCW).The PAC converts the input phase into output amplitude. Several phases toamplitude mapping mechanisms are described in [4]. More details on how toimplement a DDS are given in [5–7] that describes the implementation of DDFSby using analog interpolation method.

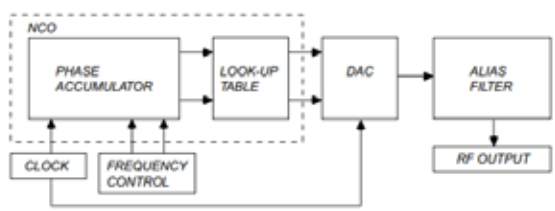

Fig. 1 Block diagram of direct digital synthesizer

3. PROPOSED DESIGN

Figure 2 shows the RTL schematic of the proposed design, and Fig. 3 shows theRTL schematic of PA. Proposed design consists of implementing a DDS usingCORDIC as a frequency–amplitude mapper block. Pipelined CORDIC is used inthe proposed design to improve the throughput to one sample per one clock cycle.

CORDIC block in the proposed design consists of 16 stages and the precision is 8bits. To improve the accuracy, the difference between the precision and number ofCORDIC stages is maintained. Mapped CORDIC is used to map the outputof CORDIC block to the entire circular coordinate system. The phase input toCORDIC consists of 16 angle bits and 2 quadrant bits. The output consists of 8amplitude bits. The input to the PA consists of 18 phase bits. These input valuesare controlled by a 2 bit 'EN' input. The PA consists of an 18-bit signed adder witha register following it. The 18-bit phase word is called FCW. The proposed designhouses three values for FCW. As the CORDIC block gives both sine and cosinevalues simultaneously, the advantage of the proposed design lies in generating the quadrature outputs. The microarchitectures of mapped CORDIC block is same asthe one mentioned in [11].

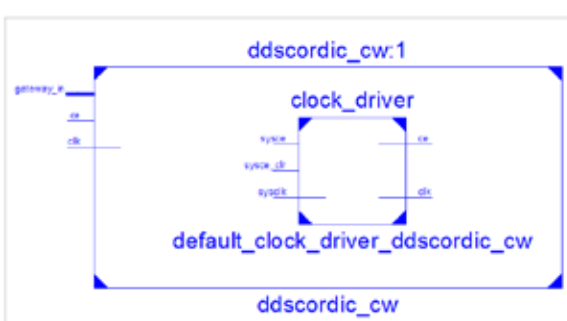

Fig. 2 RTL schematic of proposed DDFS

4. RESULTS AND DISCUSSION

The design is coded using VHDL, and the platforms considered for implementationare FPGA and ASIC. The output amplitude has a resolution of 8 bits. Thephase difference between the quadrature outputs is maintained. The design ismapped on to a variety of Xilinx FPGA families to measure the performance.Figure 4 shows the chart of device utilization of the proposed design on a varietyof FPGAs.The design is physically mapped on the Xilinx Virtex II FPGA.

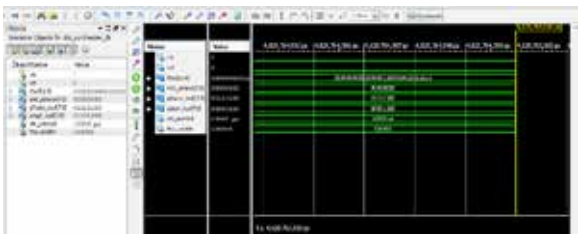

Fig.3 Simulated Result of Design

5. CONCLUSIONS

This paper reported efficient VLSI implementation of CORDIC-based DDS in FPGA design flows. CORDIC-based PAC has provided the advantage ofgiving simultaneous quadrature outputs. The amplitude resolution is 16 bits. Thedesign is physically tested on Xilinx Virtex II Pro FPGA development board. Theproposed design is mapped on to a number of Xilinx FPGA families to comparethe performance in terms of operating frequency while observing the device utilizationin each of them.

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