Research Paper

# A 1 Kw, 100 Khz Full Bridge ZVS DC-DC Converter For a Distributed Power Supply System 

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## ABSTRACT

The high voltage DC power supply require for Anode power supply of pre driver stage of RF Amplifier. Nowadays compact high voltage dc power supply is more in demand so high switching frequency is require for reduce the size of power supply. High switching frequency increase the switching loss which is minimize with the zero voltage switching. The conventional phase-shifted zero voltage switching(ZVS) DC-DC converter is applied to the many power supplies in order to reduce the voltage and current stresses of the main switching devices (MOSFETs). The ZVS method needs fairly large leakage inductance in the primary side of the high frequency transformer to get good ZVS characteristics. During the small dead time between conductions of the two bridge legs, the increased magnetizing current resonates with MOSFET output capacitance, resulting in ZVS operation. Switching losses is quite reducing with the ZVS operation in full bridge converter so efficiency of converter is increased. A crockroft-Walton voltage multiplier circuit is connected in secondary side of high frequency transformer which increases the output voltage level and rectified it. This study describes the high frequency high voltage DC power supply ( $1 \mathrm{~kW}, 100 \mathrm{kHz}$ ). Simulation is done by using PSIM software. Design equations and Simulation results are presented and discussed in briefly.
Index Terms-Crockroft-Walton Voltage Multiplier Circuit(Voltage Doubler Circuit), DC-DC Converter, High Voltage DC Power Supply, Zero Voltage Switching(ZVS).

## KEYWORDS :

## I INTRODUCTION

The proliferation of power electronics equipments with continuing success of square-wave PWM topology in switching converters can be attributed to its ease of operation. But with the demands for higher power densities, the switching frequencies are approaching 1 MHz range. At these frequencies, square-wave converters switching losses become very high leading to excessive heat dissipation. Due to smaller size of the power components, managing the excessive heat becomes a difficult problem and wipes out whatever advantages higher frequency operation provides ${ }^{[1]}$.

Various topologies have been proposed to reduce the switching losses and allow high frequency operation. All these topologies shape the switching waveforms so that at the point of switching, either the current (at turn off) or the voltage (at turn-on) is zero. Various studies have concluded that at high frequencies, zero-voltage turn-on is the most desirable feature for low switching losses. ZVS is preferred over ZCS at high frequency, the reason has with internal capacitance of switch. When the switched is turned-on a zero current but at finite voltage, the charge on the internal capacitance is dissipated in the switch. This loss does not occur if the switch turn- on at zero voltage.

The full-bridge phase-shifted converter topology ${ }^{[2-4]}$ provides a much easier solution to the wave shaping problem. Its control features are similar to regular PWM converters and it uses parasitic elements to control the switching transition for zero voltage switching. Also, the absence of resonant peaks limits the stresses on switching components.

In this paper, the main emphasis has been given up on the simulation and design of the high voltage DC power supply with 100 kHz frequency. At the first stage of this work is to study the zero voltage switching in full bridge converter and voltage multiplier circuits. Finally Design and simulation is done on $1 \mathrm{~kW}, 100 \mathrm{kHz}$ frequency DC power supply.

## II SYSTEM DESCRIPTION



Fig. 1 Basic Block diagram of High Voltage DC Power Supply

To achieve zero voltage switching in full bridge converter the leakage inductance of transformer is used and magnetizing current produce the sufficient energy to make the zero voltage switching with the parasitic capacitor of MOSFET and if the leakage inductance of transformer is less than the required inductance than external inductor is connected in series with the primary winding of the High frequency transformer to achieve the ZVS in full bridge converter to reduce the switching losses and so increases the efficiency of full bridge converter. In above Fig. 1 the output of full bridge converter is given to high frequency step-up transformer and so increase the secondary voltage of the transformer and this voltage is given to Crockroft-Walton multiplier circuit which increase the output voltage and rectified it so high voltage dc output is available.

So, to reduce the switching losses in high frequency converter the zero voltage switching(ZVS) or zero current switching(ZCS) methods are used. ZVS is more commonly used as compared to ZCS because it has following advantages.(i) No power loss due to discharging $C_{\text {oss }}$ in ZVS. (ii) No higher peak currents in zero voltage switching. (iii) High efficiency with high voltage input at high frequency. (iv) incorporate parasitic circuit and component $L$ and $C$. (v) Reduce gate drive requirements(no miller effect) (vi) Short circuit tolerant (vii) When the switched is turned-on a zero current but at finite voltage, the charge on the internal capacitance is dissipated in the switch. This loss does not occur if the switch turn-on at zero voltage.

## III CIRCUIT DESIGN

## (a) Design of $L_{R}$ and $C_{R}$ :

There are several ways to calculate the value of the resonant inductor ( $\mathrm{L}_{\mathrm{R}}=$ External series inductance + Leakage inductance) and minimum primary current required for any application. Each of these is based upon the following fundamental relationships. The resonant tank period must be at least four times higher than the transition time to fully resonate within the maximum transition time $t_{\text {max }}$ at light load.

$$
\begin{gathered}
\mathrm{T}_{\mathrm{RES}}=4 \mathrm{t}_{\mathrm{MAX}} \\
\mathrm{f}_{\mathrm{RES}}=\mathrm{I} /\left(4 \mathrm{t}_{\mathrm{MAX}}\right) \\
\omega_{\mathrm{K}}=2 \pi \mathrm{f}_{\mathrm{RES}}=2 \pi / 4 t_{\mathrm{MAX}}=\pi / 2 t_{\mathrm{MAX}}
\end{gathered}
$$

The resonant radian frequency $\omega_{r}$ is related to the resonant components by the equation. $\quad \omega_{r} r=1 /\left(L_{R} C_{R}\right)^{1 / 2}$ So, Resonant Inductor value $L_{R}=1 /\left(\omega r^{2} C_{R}\right)$

The specified MOSFET switch output capacitance $C_{\text {oss }}$ will be multiplied by a $4 / 3$ factor per the MOSFET manufactures Application Notes to approximate the correct average capacitance value with a varying drain voltage. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to $(8 / 3)^{*} C_{\text {oss }}$. Trans-
former capacitance $C_{\text {XFMR }}$ must also be added as it is not negligible in many high frequency applications, especially at lower power levels where smaller switches are incorporated.

Resonant capacitance $C_{R}=(8 / 3)^{*} C_{\text {oss }}+C_{\text {XFMR }}$
So, resonant inductor is given by $\quad L_{R}=1 /\left[\left(/ 2 t_{\text {MAX }}\right)^{2 *}\left((8 / 3)^{*}\right.\right.$ Coss + $\left.\left(_{\text {xFMR }}\right)\right]$
(b) Requirements of Stored Energy:

The energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. So,
$1 / 2 * L_{R} I_{\text {PRIIMIN })}{ }^{2}>1 / 2 * C_{R}^{*} V_{\operatorname{IN}(\text { MAX })}{ }^{2}$
Since $C_{R}$ and $V_{\text {IN }}$ are known, so $L_{R}$ can be calculated

## ( c ) Requirement of Minimum Primary Current:

The minimum primary current required for the phase shifted application can now be determined by reorganizing the previous equation. Operating below this critical current level will result in lossy transitions.
$I_{\text {PRI (MIN) }}=\left[\left(C_{R}^{*} V_{I N}{ }^{2}\right) / L_{R}\right]^{1 / 2}$
This value can be supported by calculating the average current required to slew the resonant capacitor to the full rail voltage. Although this figure will be lower than $\mathrm{I}_{\mathrm{P}(\mathrm{MIN)}}$, it can be used to confirm the calculations.
$I_{\text {R(AVG) }}=C_{R} V_{I N} / T_{\text {MAX }}$
Obtaining the necessary amount of primary current can be done in several ways. The most direct approach is simply to limit the minimum load current to the appropriate level. One alternative, however, is to design the transformer magnetizing inductance accordingly. Also assisting the magnetizing current is the reflected secondary inductor current contribution which is modeled in parallel.

## IV SIMULATION RESULT

Simulation is carried out by Using PSIM Software and following parameters are taken for the Design and Simulation as shown in Table I:

Table I: Design Parameters for Simulation

| Supply Voltage | 325 Peak |
| :--- | :--- |
| Supply Frequency | 50 Hz |
| MOSFET output Capacitance | 800 pF |
| Resonant Inductor | 18 uH |
| Resonant Capacitance | 2800 pF |
| Capacitor of Multiplier circuit | 500 nF |
| Crockroft-Walton Multiplier Circuit | 10 Stage |
| Transformer ratio | $1: 2$ |
| Switching Frequency | 100 kHz |
| Output Resistance | $100 \mathrm{k} \Omega$ |



Fig. 2 Ten Stage Crockroft - Walton Voltage Multiplier Circuit


Fig. 3 Zero Voltage across the switch before the gate pulse is ON


Fig. 4 Each stage Output Voltage of Crockroft Walton multiplier stage.


Fig. 5 Output Current of proposed High Voltage DC Power Supply

Fig. 4 shows the zero voltage switching is achieved before the gate pulse is ON. Here gate pulse is ON when voltage across the switch is zero so switching loss is reduced and so efficiency of the power supply is increase. Fig. 5 shows the output voltage of power supply for each stage output voltage is $1 \mathrm{kV}, 2 \mathrm{kV}, 4 \mathrm{kV}, 6 \mathrm{kV}, 8 \mathrm{kv}$ and 10 kV achieved. Fig. 6 shows the output current 100 mA is achieved of high voltage dc power supply.

## VI conclusion

The compact high voltage dc power supply can be design with the proposed topology with high switching frequency. However the switching losses will increase with high switching frequency. Switching losses are reduced by using proposed ZVS technique, and therefore the efficiency of power supply is increased. To achieve Zero Voltage Switching with phase shifted PWM, the leakage inductance of transformer should be taken high and give a sufficient dead band between the two lag switches but at the same time duty cycle is decrease which is the demerit of ZVS with phase shifted PWM full bridge converter. Simulation result shows that zero voltage switching achieved and distributed power supply of 1 kW with high frequen$\mathrm{cy}(100 \mathrm{kHz})$ with different output voltage level is available for distributed power supply system.

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