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Implementation of 16:1 Multiplexer In Low Power Quaternary Logic Look Up Table

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ABSTRACT

These Most of the chip area in FPGA is consumed by Lookup tables (LUT) and configurable routing switches. Reduction in power consumption can be achieved by scaling down interconnections through MVL. Closer levels in MVL reduces power required for level transition. By using Quaternary logic we can reduce the interconnections, as each circuit wire in quaternary logic can carry the same information as that of two wires in binary logic. In this paper, we design a low power look up table, based on quaternary logic and implement a 16:1 multiplexer using it. Cadence virtuoso GPDK 180nm technology is used to design the look up table in standard CMOS with power consumption of 88µW at 500 MHz frequency.

KEYWORDS : Quaternary Logic, Lookup Table, Standard CMOS technology, Multiple Valued Logic

INTRODUCTION

In CMOS digital circuits, dynamic power consumption depends on power supply by which it is driven and total capacitive nodes it drives. Implementing these circuits in smaller area and smaller operating voltages and higher frequencies is all about VLSI deigns.

P_D αCV_DD^2

However, Capacitance also includes interconnecting wires among logic circuits. In recent studies it has been concluded that routing capacitance is consuming more power than transistor switching. It is also responsible for delay in recent VLSI designs. This is more serious factor in programmable logic devices. Amongst programmable devices in VLSI CMOS technologies Field programmable logic devices use more configurable cables which lead lot of power and area consumption. In most of recent FPGA designs 70% of power consumption is used to configure connections among logic blocks. Due to special feature as re-configurability FPGAs are important in modern times whereas ASIC design is costlier processor and takes longer design time. Using multiple valued logic in CMOS designs can reduce power consumption. Power consumption also includes voltage difference between logic levels. By using MVL difference between logic levels comes down and hence power consumption also comes down.

P_D α CV_DD V_av

The motivation in using Multiple-valued logic in designing FPGAs has started to reduce the area of conventional binary FPGAs, which indeed are in large sizes. FPGAs are rich source of look up tables and routing switches. Having more number of logic blocks is a key feature of an FPGA and hence interconnect network between them takes considerable amount of chip area. Quaternary logic can reduce the area of an FPGA as a quaternary signal can carry the information twice that of a binary signal. As number of interconnects reduces capacitance related to parallel interconnects reduces. Power required for level transition can also reduce. Hence there is a scope to reduce power consumption of an FPGA using quaternary logic design.

Quaternary logic has been used previously by current mode logic and by non-standard multi threshold CMOS in which power consumption is more. We use a standard technique called three different thresholds by which power consumption can be lowered.

Usage of FPGAs is growing tremendously from past few years. This growth in usage is because they can implement any number of complex logic functions, any number of times. It uses huge resource to be this flexible. Power and area can be improved in good numbers by using quaternary LUT's than binary LUT's. Hence, reduction of wiring, routing switches can be obtained using quaternary logic instead of binary, which in turn reduces the area of an FPGA.

Current mode logic in CMOS circuits design has become popular in recent times. They are interesting and can have many applications in DSP. Current mode MVL circuits have a reference current value and use its multiples as logic levels for computing whereas voltage mode MVL a reference voltage to divide logic levels. Generally they use supply voltage as reference. Designs using current mode logic become complex rather than voltage mode. Feed back in current mode logic is low compared to voltage mode logic which makes them less popular.

Using nonstandard multi-threshold technique consume more power and may result in improper signal outputs. Replacing transmission gates for pass transistor will prevent disturbance in signal shapes with increase in power consumption. Signal shape can be conserved using boot strapping switch. In FPGA design, dynamic power is also influenced by interconnect capacitance in addition to switching activity. Huge routing in FPGAs induce parallel line capacitance.

QUATERNARY LOGIC AND LUTs

The main aspect of the paper is to design a low power quaternary logic look up table in CMOS standards. Routing network in an FPGA can be reduced by using multiple-valued logic. LUTs and CLBs consume most of the area in FPGAs. Using quaternary logic area of routing network in an FPGA reduces as a quaternary signal can carry the information twice that of a binary signal. Dynamic power of circuit depends on level transition, circuit capacitances and frequency of operation. Power consumption also reduces in quaternary logic as power for level transition is low and line capacitance reduces. A quaternary logic look up table has a quaternary to binary decoder, a 16: 1 switch level multiplexer and a clock boosting switch.

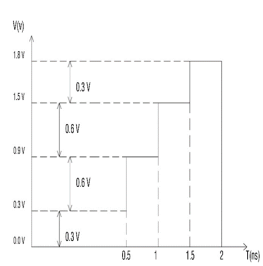

Fig 1: Step signal or quaternary signal

Input quaternary signal is decoded by quaternary to binary decoder and is fed to multiplexer as a selection line. The converted binary signal turns on switch in the multiplexer and its corresponding configuration is mapped to output of LUT. As signal is quaternary signal, to avoid loss in signal strength we design a clock booster switch and use it in multiplexer.

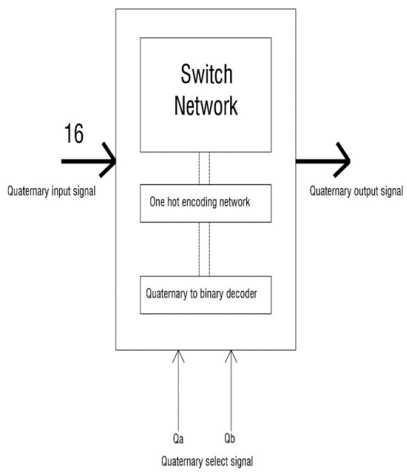

Fig 2: Quaternary logic look up table block

The figure shown above is the block diagram of look up table design with inputs two select inputs, 16 primary inputs and 1 output.

Firstly, the aim is to design a 2:16 quaternary to binary decoder. As the input to decoder is 2, we may say it a 2-bit quaternary to binary decoder. The source to generate this quaternary input signal is not readily available in cadence and hence we generate this using piece wise linearity. A quaternary signal is a step signal with specified logic levels. The step signal shown in Fig: 1 above has to be converted to binary signal by decoder. This step signal voltages are divided in to several voltage levels which are defined as in below Table: 1. we choose quaternary logic and so we need 4 levels of voltage signals.

Table-1

Logic Table

Quaternary logic levels	Reference voltage levels	Voltage standard
Logic 3	Vdd	1.8V
Logic 2	5/6*Vdd	1.5V
Logic 1	3/6*Vdd	0.9V
Logic 0	1/6*Vdd	0.3V

At higher frequencies the quaternary signal resembles an analog signal and hence decoder may also be considered as ADC. This circuit can be constructed using three inverting self-referenced comparators.

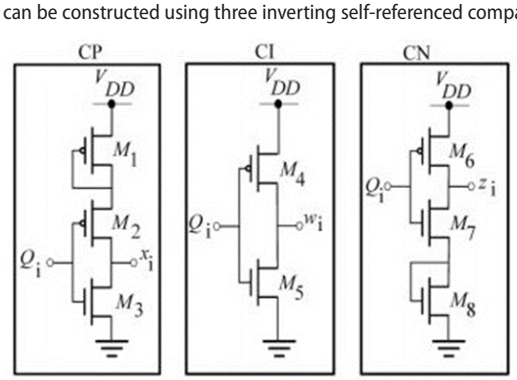

Fig 3: Quaternary to binary decoder

The circuits shown above CP, CN, CI are applied with step input and three digital signals are collected at the output x, y, z respectively. CP has more P resistance than N resistance whereas CN has more N resistance than P resistance. These differences in CP and CN is responsible for stronger 0 and stronger 1 at the output signals correspondingly. CI is an inverter circuit. These circuits are designed in standard CMOS using 3 different Vth technique. Here 3 kinds of MOSFETs are used with different threshold voltages. These MOSFETs are readily available in GPDK's library. The MOSFET with high threshold voltage is known as HVT, low threshold voltage is known as LVT and with standard threshold voltage is known as SVT.

Threshold voltage of a MOSFET:

$$V_t = V_{fb} + 2\emptyset_b + \frac{\sqrt{2\epsilon_{si} q N_a (2\emptyset_b + |V_{sb}|)}}{C_{ox}}$$

$$\text{Here} \quad V_t \alpha \frac{1}{C_{ox}} \alpha\, t_{ox}$$

Hence threshold voltage of a MOSFET is directly proportional to its Gate oxide thickness. Oxide thickness is a factor only in control of Fabricators. So fabricators give various MOSFET models in Process Design Kits (PDK).

MOSFET Current Equation:

$$I_{ds} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_t)^2$$

$$I_{ds} \alpha C_{ox} \alpha \frac{1}{t_{ox}}$$

Hence Current in MOS transistor is inversely proportional to thickness of oxide which implies HVT consumes less current and is slower compared to LVT. This also implies that HVT devices are slower than LVT models but advantageous in case of leakage current.

Using these MOSFET models decoder has been designed and observed that they provide weak 0 and weak 1 which is compensated by passing them through inverter circuitry. The output of this decoder followed by an inverter is plotted as waveform later in the document. Design of one hot encoding circuitry is next step in implementation of look up table. Designing this circuitry in nand gates can bring down delay and power consumption. To design a one hot encoding response of a circuit it should act as following decoding logic

Table-2

One Hot Combinatorial Function

Qa	Qb	Xa	Ya	Za	Xb	Yb	Zb	Switch
0	0	0	0	0	0	0	0	vds(1)
1	0	1	0	0	0	0	0	vds(2)
2	0	1	1	0	0	0	0	vds(3)
3	0	1	1	1	0	0	0	vds(4)
0	1	0	0	0	1	0	0	vds(5)
1	1	1	0	0	1	0	0	vds(6)
2	1	1	1	0	1	0	0	vds(7)
3	1	1	1	1	1	0	0	vds(8)
0	2	0	0	0	1	1	0	vds(9)
1	2	1	0	0	1	1	0	vds(10)
2	2	1	1	0	1	1	0	vds(11)
3	2	1	1	1	1	1	0	vds(12)

0	3	0	0	0	1	1	1	vds(13)
1	3	1	0	0	1	1	1	vds(14)
2	3	1	1	0	1	1	1	vds(15)
3	3	1	1	1	1	1	1	vds(16)

There are two types of encoding generally, they are hot encoding and cold encoding. Hot encoding is one in

There are two types of encoding generally, they are hot encoding and cold encoding. Hot encoding is one in which at a time only one of the outputs is high and remaining stay at logic zero or low where as cold encoding is in which one of the outputs is at low and remaining are at logic one. Generally one hot encoding is preferred technique as it consumes low power than cold encoding technique. Voltage doubling switch is used to pass the step signal through it, which is controlled by this one hot signal generated.

QLUT IMPLEMENTATIONS

In this paper we design a Quaternary to binary decoder, a 16:1 switch level multiplexer and a clock boosting switch which are main building blocks of Quaternary logic look up table.

In this second module of the paper we design a 6:16 one hot encoding circuit. The output of quaternary to binary decoder is applied to a one hot encoding logic network and collected encoded circuit response at the output. Here one hot encoding network has been used second module by which only one switch amongst 16 can be turned on. This implementation is done using three and four input nand gates by dividing the logic table in to 4 sub circuits based on one of the quaternary inputs. A set of nand network has been shown in following figure:

III) VOLTAGE DOUBLING SWITCH:

Voltage doubling switch is used in circuit to control pass gate to replicate various voltage levels in quaternary signal.

To understand voltage doubling in this circuit consider when input CBSin is at logic 1, forcing output of the inverter to logic 0. Hence bottom plate of capacitor is at virtual ground and top plate starts charging as M4 (NMOS) turns on, and pulls down node voltage to ground which leads M0 (PMOS) to turn on.

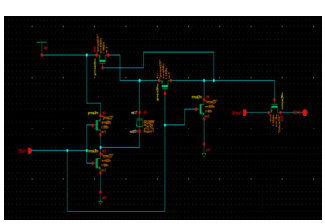

Fig 4: Voltage doubling switch

Hence top plate of capacitor is charged to supply and when input CBSin turns to logic 0, inverter output flips to logic and charges capacitor to 2 times of supply voltage. MOSFET M5 (NMOS) is a pass transistor whose drain input is quaternary signal input and at source we collect quaternary output. While designing this circuitry we used HVT model which has less leakage to pass supply and quaternary signal, whereas LVT model as inverter charging bottom plate of charger.

SIMULATION RESULTS AND ANALYSIS

The simulation results are going to be observed in spectre simulation window.

Once after drawing the schematic in virtuoso schematic editor, we have simulated it using analog design environment of cadence. Inputs of frequency 500MHz and 125MHz are applied to the decoder and outputs of decoder fed to one hot encoding circuit and its outputs are observed. The source Vpwl is used to generate step waves with frequencies 500MHz, 125MHz which can be seen as symbol source.

The simulation result as shown below:

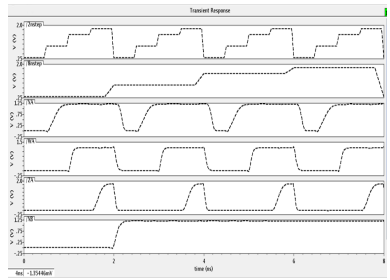

Fig 5: output waveform 1

In the above waveform we observe that input quaternary logic signal has been converted in to binary logic with bad slew. This binary signal is applied to one hot encoded nand network to obtain following response. Here we can observe at any time instant only one signal is going low. As signal is going low it does not mean to be cold encoding but we avoided inverter delay to increase operational frequency.

Obtained one hot signal is applied to voltage doubling switch whose selection lines are quaternary, inputs are quaternary and attained output is also quaternary.

Table-3
Comparision Table

Parameter	This Work	[4]
Number of input	2	2
Technology node	GPDK 180nm	TSMC 180nm
Design Technique	3 Diffrent Vth used for LUT	3 Diffrent Vth
Voltage Supply	1.8 V	1.8 V
Frequency	500 MHz	500 MHz
Load capacitance	2.5fF	2.5fF
Transistor count	320	84
Power Consumption	88 µW	155 µW

CONCLUSION:

In this paper, we designed a Quaternary logic based lookup table using combinational logic in standard CMOS structures. This is done using self – referenced voltage mode comparators which convert quaternary signal to binary. A one hot encoding circuit and high frequency operational boot strap switch are also used to reduce power consumption. This look up table was tested as multiplexer for quaternary logic and can be used as valid solution for routing complexity in FPGAs.

REFERENCES

[1] K. Current, "Current-mode CMOS multiple-valued logic circuits," IEEE J. Solid-State Circuits, vol. 29, no. 2, pp. 95–107, Feb. 1994.

[2] R. da Silva, C. Lazzari, H. Boudinov, and L. Carro, "CMOS voltage mode quaternary look-up tables for multi-valued FPGAs," Micro electron. J., vol. 40, no. 10, pp. 1466–1470, 2009.

[3] D. Brito, J. Fernandes, P. Flores, and J. Monteiro, "Design and characterization of a QLUT in a standard CMOS process," in Proc. IEEE 19th ICECS, Dec. 2012, pp. 288–291.

[4] D. Brito, G. Rabuske, R. Fernandes, Paulo Flores, Jose Monteiro, "Quaternary Logic Lookup Table in standard CMOS," IEEE transactions on very large scale integration.

[5] Singh, A., Marek-Sadowska, M.: Efficient circuit clustering for area and power reduction in FPGAs. In: FPGA '02: Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays, New York, NY, USA, ACM (2002) 59–66.

[6] Cunha, R., Boudinov, H., Carro, L.: Quaternary look-up tables using voltage-mode CMOS logic design. ISMVL 2007. 37th International Symposium on Multiple Valued Logic (May 2007) 56–56.

[7] Cadence Design Systems Inc.: Virtuoso spectre simulator user guide. (2010).

[8] Li, F., Lin, Y., He, L., Chen, D., Cong, J.: Power modelling and characteristics of field programmable gate arrays. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 24(11) (Nov. 2005) 1712–1724