Research Paper Engineering

Proficient 15-Bit Flash ADC Design Using Wallace Tree Adder

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ABSTRACT

The signals in this present reality are analog in nature for instance light, solid, video and so on. In request to accomplish digital signal, we have to change over the analog signal into digital form by utilizing a circuit called analog-to-digital converter. The interest for the converter is situated on area, speed, power of the converters. In request to accomplish these optimization's we are designing a comparator, a Wallace tree adder and an inverse Gaussian function. Here, speed can be improved by developing an analog comparator from two cross-coupled 3-input digital NAND gates. To reduce power utilization we are using Wallace tree adder, which is normally used for high speed and efficient one's addition. Here, the fundamental reason for inverse Gaussian function is to take out the noise present in the output furthermore to reconstruct the digitalized signal into its original form. So as to outline a flash ADC, all blocks including the comparators, the ones adder, and the piece wise inverse Gaussian function are designed in Verilog HDL. To implement this architecture on FPGA we are using Vivado 2014.2.

KEYWORDS : Comparator, Wallace Tree Adder, Inverse Gaussian Function, Wallace Tree Adder, Cross-coupled NAND Gates, Inverse Gaussian Function.

INTRODUCTION

An ADC is a mixed-signal framework with an analog front-end and a digital back-end. Ordinarily, ADCs depend intensely on great analog design, to be specific careful matching, layout, and liner circuits. As circuits scale into deep submicron, designing highly linear circuit segments gets to be progressively troublesome. Accordingly, an ADC architecture that can rely less on linear circuits is desirable.

The most fundamental segment of an ADC is the comparator. The element eventually does the interpreting from the analog world to the digital world. The circuits upstream from the comparator have a tendency to be very analog, and those downstream, digital. The digital circuits open up signals the distance to the rails, so linearity is not essential, just delay matters. Due to their naturally low affectability to noise and physical layout, digital circuits lend themselves to automated synthesis. In request to minimize analog circuit necessities, it is proper to design an architecture that is exceptionally digital.

Subsequent to the comparator characterizes the limit is in the middle of analog and digital domains, the flash ADC design will be considered, as it places the comparator as near the analog information signal as could be expected under the circumstances. On the off chance that there is no pre-amplification, the main analog segments in a conventional Flash ADC are the analog voltage references and the comparators.

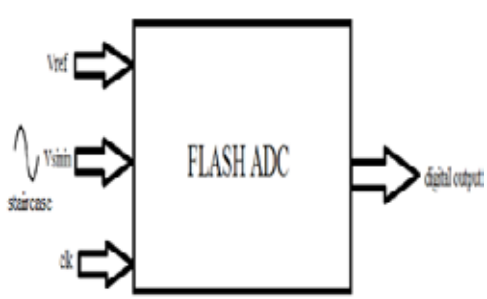

Figure 1: Basic block diagram

Typically the references are employed by using 0.13µm CMOS copper technology [1], by using stochastic quantization methods [2] or by employing a large number of 1-bit quantizers operating in parallel with additive noise and a novel probability density transform [3].

Another approach [4] is that by connecting many comparators in parallel, reference ladder is avoided by allowing random offsets to set individual trip points. This technique is proposed to improve transfer function linearity. To improve the design of flash type converter several architecture have been proposed such as two- stage architecture [5] [6] another technique Threshold Inverter Quantization [7]. This technique eliminates the use of the resistor ladder and reduces the complexity of the converter.

The overall architecture is discussed in Section II. Section III discusses the operation of an analog comparator that is constructed from standard digital NAND gates. Section IV deals with the DSP block. The results of the said test chip are presented in Section V.

OBJECTIVE

In this paper, the main objective is to design a flash ADC by using verilog HDL. The advantage of using verilog HDL is to generate physical layout directly after conventional digital synthesis and place-and-route as generating layout by using analog components is a time taking process. Here, we are reducing the design complexity of comparators by using standard digital cells. As in the reference paper they used normal adder for reconstruction of analog signal from the digital output. In this project, we are using Wallace tree adder for efficient and high speed addition.

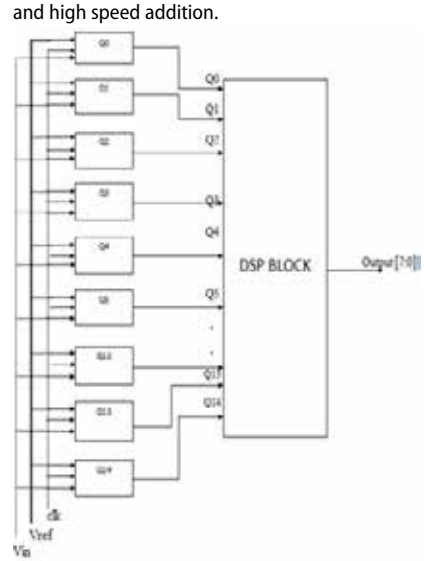

Figure 2: Architecture of Flash ADC

SINE WAVE GENERATION

The sine wave or sinusoid is a numerical curve that depicts smooth repetitive oscillations. It is named after the function sine, of which it is the graph. It happens frequently in pure and applied science, and also material science, designing, signal processing and numerous other fields. The sine wave is vital in physical science since it holds its wave shape when added to another sine wave of the same frequency and arbitrary phase and magnitude. It is the main intermittent waveform that has this property. This property prompts its significance in Fourier analysis and makes it acoustically one of a kind.

Table 1. Specifications of Input Signal

Input Signals	Vref	Vsinin
Input Range	7V	5V
Input Frequency	2MHz	1.6MHz

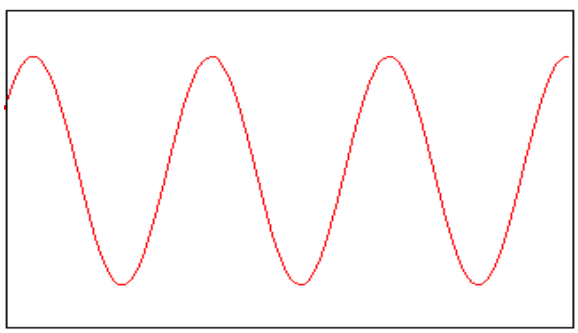

Figure 3: Sinusoidal waveform

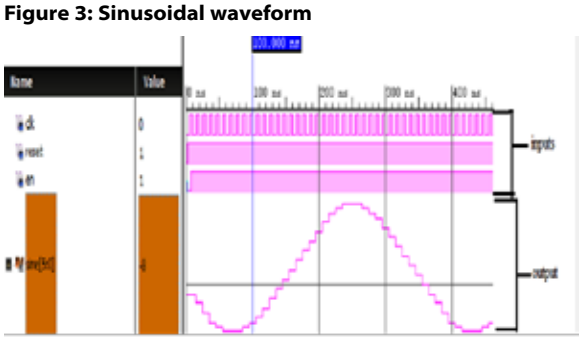

Figure 4: Simulation result for sine wave

COMPARATOR

In a routine Flash ADC, the information signal is associated to the inputs of a group of comparators. The threshold of each comparator is set correctly, by some kind of reference ladder, such that all comparator thresholds are similarly divided by 1 LSB. As a general rule, there is likewise a random balance in each comparator that, in actuality, straightens out each comparator threshold by a random amount. This random amount, because of random mismatches can be thought to be a Gaussian circulation with a mean of zero.

With a specific end goal to synthesize a Flash ADC from Verilog code, there are a couple key changes that should be made to the architecture. Above all else, the resistor ladder must be removed. The differential input is then associated specifically to the data of the greater part of the comparators. Subsequent to there are no more explicit voltage references, this architecture relies on upon the virtual voltage references that exist as comparator due to random mismatches. In the event that the mismatch is too small, then the input signal range will likewise be exceptionally small, so small comparators are really favored.

Figure 5 : 3-input NAND gate

Upon perception, the schematic of the transistors inside a CMOS NAND gate nearly look like portion of a timed simple comparator. By associating two NAND gates together, a simple analog comparator is made if the basic method of the data is sufficiently high to guarantee that the PMOS transistors associated with the data are in the cutoff district of operation. At the point when the clock is low, both yields are reset to the positive supply rail. At the point when the clock goes high, the yields will start to release through the three arrangement NMOS devices.

The release rate relies on upon the capacitance on the yield hub and the current through the three series devices. Since one of the series devices is associated with the simple data, the discharging current is proportional to input. When one of the yields releases to underneath a PMOS limit voltage, the cross-coupled association makes positive input that causes the comparator to drive the yields the distance to the supply rails. Executing such a comparator should be possible by unequivocally referencing the standard library cells in the RTL Verilog code.

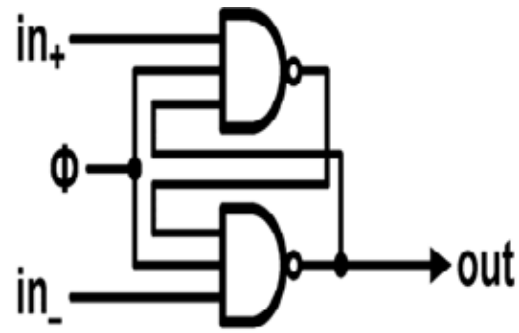

Figure 6: Analog comparator designed from standard digital cells

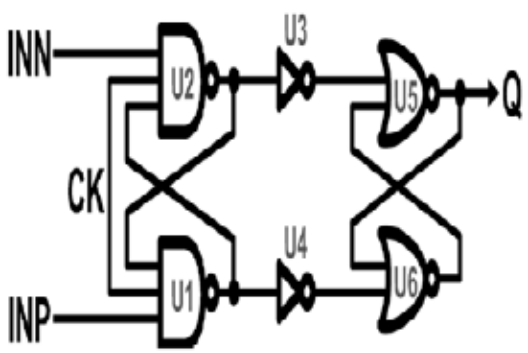

Figure 7: Gate- level schematic representation of analog comparator

In this sample, a static SR-latch is added to the yield of the comparator. The SR-latch holds the yield information substantial while the comparator is reset. The SR-latch input is buffered with inverters to reduce a memory-impact on the comparator because of the SR-latch. Despite the fact that this circuit is inherently good with digital synthesis, the synthesizer will expect that the circuit is really a digital one, and will attempt and upgrade it by supplanting a few of the gates or changing the circuit completely while keeping up the same advanced capacity. This advanced optimization might render the circuit non-functional from a simple point of view.

DSP BLOCK

Wallace Tree adder

The last block of the Flash ADC is the rationale that samples the comparator yield and puts the group of 1s into an arrangement readable by a FPGA or micro processor. A common Flash ADC intended for linearity and exact yield without adjustment may have thermometer code to binary converter. This will change over the raw yields into a binary number. This outline is typically accepting no bubble codes and all trip points composed in a row. Bubble codes will be codes in the thermometer string that ought to be 1 however are zero due to

comparator offset. This ADC will in all probability be bubble codes and different mistakes in our yield, we will utilize a adder to count the ones. The adder that will be utilized will be a Wallace tree adder. Unlike all like typical Flash ADC encoders, this method will offer the blunder rectification and suppression without the utilization of expansion of NAND gates with the bubble codes. This configuration might be moderate and need pipe-lining to enhance its execution.

There are numerous situations where it is wanted to include more than two numbers together. The clear method for including m numbers (all n bits wide) is to include the first two, then adds that entirety to the following utilizing falling full adders. This requires an aggregate of m − 1 increases, for an aggregate door postponement of O(m lg n) (accepting look-a-head convey adders). Rather, a tree of adders can be shaped, taking just O(lg m · lg n) door delays. A Wallace tree adder includes n bits to deliver a total of log2n bits.

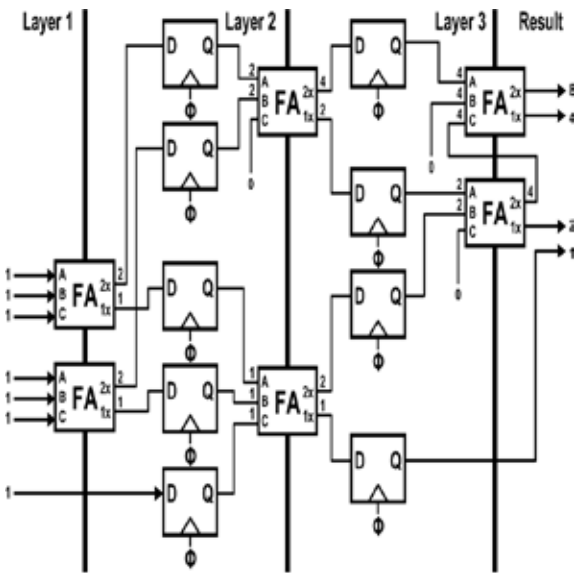

Figure 8: Block Diagram of Wallace Tree Adder

Inverse Gaussian Function

A functional piece with an inverse Gaussian CDF transfer function is put after the flash ADC output to linearize the output. The inverse Gaussian piece can be actualized as either as a lookup table or a digital mathematical function. There are grave disadvantages in executing this as a lookup table on hardware. A lookup table is a huge hardware requirement since it is implemented as a memory that should have the capacity to output as quickly as the ADC. Depending upon the precision that we are outlining, a piecewise linear approximation of an inverse Gaussian CDF is adequate.

RESULTS

This section deals with the schematic designs after the implementation and also with the performance results.

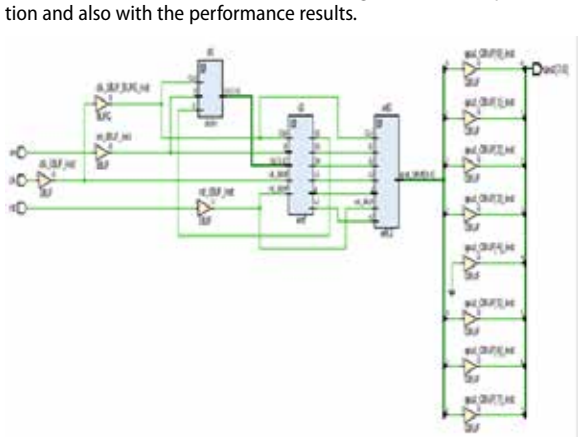

Figure 9: Schematic View of Top Module

Table 2: Performance Analysis

Parameters		Reference Paper	Proposed Work
Complexity		More	Less
Area	No. of slice Flip-Flops	13	9
	No. of 4-input LUT's	20	8
	No. of Occupied Slices	18	10
	No. of bonded IO's	12	12
Delay		5.32ns	4.22ns
Power Consumption		1.63W	1.275W

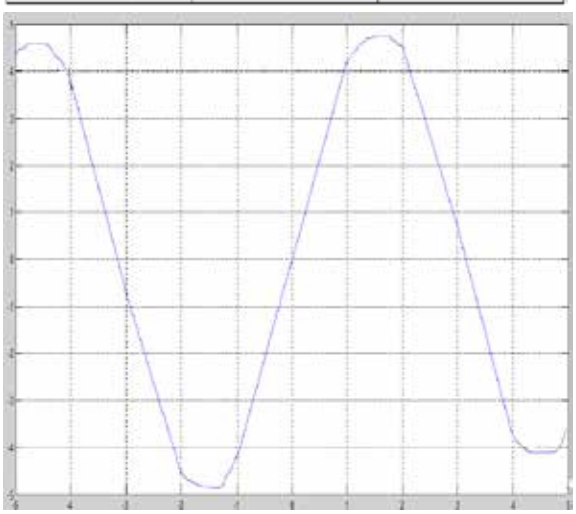

Figure 12: Reconstruction of input signal

CONCLUSION

In this paper, the principle aspect is to design a Flash ADC using Standard Digital cells. The advantage of using verilog HDL is to create physical layout straightforwardly after the conventional digital synthesis and place-and-route. As generating layout by using analog components is a time taking procedure. The interest for the converter is oriented on area, speed, power of the converters. To accomplish these enhancements we are designing a comparator, a Wallace tree adder and an inverse Gaussian function. These three components are designed and simulated using Vivado Design Tool and executed on FPGA.

Implementing the split-ADC calibration procedure minimizes analog complexity and empowers simply background calibration. This model IC demonstrates that combining an ADC totally from Verilog is possible. A comparator that is designed as two cross-coupled 3-input NAND gates has been shown to work successfully as a genuine analog comparator. By using a piecewise linear approximation of the inverse function of a Gaussian CDF, 90% of the comparators of a single Gaussian group as turned into a successful uniform appropriation to the accuracy required. The outcome is a really all digital ADC with the main analog data being the input signal.

ACKNOWLEDGEMENT

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