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THE EVALUATION AND SELECTION OF THE THREE-DIMENSIONAL INTEGRATED CIRCUITS THROUGH-SILICON VIA (TSV) PACKAGE TECHNIQUES

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ABSTRACT In the past decade, high performance, small form factor and low cost have become basic requirements for portable electronic devices. Instead of the traditional dimensional scaling techniques (e.g., shrinkage from 90 nm to 65, 45, and 28 nm), the multiple-chip package (MCP) is one of the alternatives to achieve these goals. Three-dimensional (3D) packaging is one of the main MCP techniques that has emerged in recent years. 3D integrated circuits (3D IC) can achieve smaller chip area with lower power consumption than other MCP solutions. Thus, 3D ICs can better meet the requirements of portable devices like smartphones, tablet PCs, and digital cameras which require fast time-to-market, low power consumption, miniaturization and high data transmission bandwidth. Various 3D IC techniques are available, such as the stacked-die with TSV and package-on-package stacking. The TSV technique was adopted and commercialized in Micro Electro Mechanical Systems (MEMS) and Complementary Metal Oxide Semiconductor (CMOS) Image Sensors (CIS) years ago. Various TSV techniques are currently available. TSVs can be formed from the front side of the semiconductor wafer using via-first, via-middle, or via-last processes. In addition, TSVs can be formed using a via-last process from the backside of the wafer. The selection of TSV technique depends heavily on the manufacturers and system applications. For example, the TSV techniques being applied for the integration of heterogeneous semiconductor devices, e.g., dynamic random access memories (DRAMs) and logic devices can differ from those used for the integration of homogenous devices, e.g., the integration of smaller-capacity DRAMs to achieve a larger-capacity one. Furthermore, the TSV techniques being provided by chip makers or packaging houses can differ. Very few researchers have studied the evaluation and selection of 3D IC TSV techniques, despite their importance. In order to resolve this problem, a Decision Making Trial and Evaluation Laboratory (DEMATEL) -based novel multiple-criteria decision making (MCDM) method with the Analytic Network Process (ANP) will be proposed for evaluating and selecting the 3D IC TSV techniques. An empirical study based on the 3D IC TSV technique selection will be used to verify the feasibility of the proposed analytic framework. Based on this technology assessment framework, the via-middle of 3D IC TSV technique was chosen as the best solution given the current situation of the semiconductor industry. Of the 20 assessment criteria, "partner risk", "long-term strategic relationship", and "heterogeneous integration" were the three most significant factors. In the future, the proposed technology assessment framework can be applied for the selection of other emerging technologies.

KEYWORDS : 3D integrated circuits (3D IC), Through-Silicon Via (TSV), multiple criteria decision making (MCDM)

INTRODUCTION

Performance and productivity of micro-electronics have increased continuously over more than four decades due to the enormous advances in lithography and device technology. Downscaling of semiconductor devices is the traditional way to enhance the efficiency of semiconductor device, but the research and development required to continuously shrink the line width are extremely expensive. Only a few companies can afford such costs for process technology migration [1]. Furthermore, industry experts have started to question whether the so-called "More Moore" development alone will be enough to overcome the predicted performance and cost problems of future IC fabrication [2]. The ITRS roadmap also predicted that development of the semiconductor industry will be dominated by shrinking transistor gate dimensions, which alone would not be enough to overcome the performance and cost problems of future IC fabrication [3]. In general, line width miniaturization and device shrinkage are too expensive to be affordable by most semiconductor manufacturers. The very expensive device shrinkage technique also is not enough to achieve the performance and cost goals. Alternatives to resolving the above-mentioned performance and cost gaps are very necessary for meeting the needs of electronic industry development.

The 3D stacking of dies interconnected by the Through-Silicon Via (TSV) technique has been recognized by semiconductor experts as a key technology to resolve the above-mentioned performance and cost problems and to extend the momentum of Moore's Law into the next decade [4]. Demands for the TSV have been driven by the need for 3D stacking to shorten interconnection length, increase signal speed, and reduce power dissipation. The increasing demand for reduced power consumption in new and more advanced electronic products with a smaller form factor, superior functionality and performance at a lower overall cost has driven the semiconductor industry to develop more innovative advanced packaging technologies [5]. In the billion transistor era, 3D stacking offers an attractive solution for the difficulties resulting from large-scale design complexities. Moreover, 3D stacking can benefit performance, power, bandwidth, footprint, and heterogeneous technology mixing [6]. The next generation of small form factor (SFF) microsystem technologies can only keep up with increased functionality and performance demands by using the third dimension [7].

In comparison to conventional wire-bonded interconnects, TSVs promise to increase the interconnect bandwidth and performance while lowering power dissipation and overall manufacturing cost [8]. The integration of 3D technologies will enable performance, form factor and cost requirements of the next generation of electronic devices [9]. Applications may range from miniaturization of portable electronics like image sensors and cell phones to power-efficient, high-performance computing solutions such as servers and super computers [10]. All the key enabling technologies, such as TSV, μ-bumping, thin wafer handling, bonding, and fine-pitch RDL fabricated on both sides of the wafer, need to meet stringent yield and reliability requirements without sacrificing system performance [11]. Furthermore, 3D IC TSV interconnects are the most appropriate solution for providing the wide I/O interface between logic and memory that is required for future mobile processor applications and high-performance ASICs [12].

Very few researchers have studied the methods for evaluating and selecting 3D IC TSVs, despite their importance. In order to address this gap in the literature, a Decision Making Trial and Evaluation Laboratory (DEMATEL) technique-based novel multiple-criteria decision making (MCDM) method with the Analytic Network Process (ANP) will be proposed for evaluating and selecting 3D IC

TSVs. An empirical study on 3D IC TSV technique selection will be conducted to verify the feasibility of the proposed analytic framework. Opinions of experts in the related domains of semiconductor device manufacturing and marketing will be introduced to help select the most suitable 3D IC TSV technology. The technology can be used in future 3D IC TSV applications.

The remainder of this paper is organized as follows. Section 2 introduces the concepts of technology assessment and 3D IC TSV. Section 3 introduces the Modified Delphi, DEMATEL, and ANP methods. Then, in Section 4, an example is provided to illustrate the analytic framework, and a DEMATEL-based network process will be used to derive the dimension and criteria weights. Then, suitable 3D IC TSV technology classes will be selected based on the aggregated performance scores. A discussion will be presented in Section 5. Section 6 will conclude with observations, conclusions and recommended directions for further study.

LITERATURE REVIEW

Technology Assessment

Technology Assessment (TA) has been a growing field of management study for the past four decades. An increasing number of studies have been carried out over the years contributing to the development of TA literature [13]. TA has elsewhere been grouped with science and technology foresight and policy evaluation as different tools for strategic intelligence [14]. Four characteristics of Renewable Energy Technologies (RETs) were found to directly motivate strategy and policy considerations: Site Specificity, Inter-mittence, Resource Intensity, and Technology Maturity [15].

Musango [16] conducted the framework, termed system approach to technology sustainability assessment (SATSA), integrates three key elements: technology development, sustainable development, and dynamic systems approach. The article then demonstrates the framework of incorporating the system dynamics methodology in energy technology assessment theory and practice within the context of sustainable development. [17] developed the subordinate manufacturing system objectives cost, quality, flexibility and sustainability will be used as top-level technology-related objectives. [18] proposed the experience of operationalizing of a framework for technology selection, which was based on the structure provided by the framework. They reports on how theoretical concepts presented in the framework relate to 'real-life' technology selection considerations. Farooq and O'Brien [19] concluded a structured analytical approach for selecting a manufacturing technology. A framework consisting of six integrated steps is proposed by considering the growing importance of supply chains in manufacturing organizations. [20] presented a novel assessment process that aims to evaluate and prioritize candidate technologies according to their innovation potentials by considering commercialization, imitation and trendiness factors all together.

3D IC TSV

One of the hottest topics in the semiconductor industry today is 3D Packaging using Through Silicon Via (TSV) technology [5]. 3D integration technologies can be grouped into following distinct technology approaches: (i) 3D-monolithic IC integration, (ii) 3D stacking of IC-dies, wafers and packages, and (iii) 3D integrated packaging [7]. 3D integration consists of 3D IC packaging, 3D IC integration, and 3D Si integration. They are different and in general the TSV separates 3D IC packaging from 3D IC integration and 3D Si integration since the latter two use TSV but 3D IC packaging does not. TSV (with a new concept that every chip or interposer could have two surfaces with circuits) is the heart of 3D Si integration and 3D IC integration.[21]

The enabling Three-dimensional (3D) chip integration technology elements include: (i) through-silicon-vias (TSV) with thinned silicon wafers, (ii) fine pitch wiring, (iii) fine pitch interconnection between stacked die, (iv) fine pitch test for known-good die, and (v) power delivery, distribution and thermal cooling technology [10]. Through Silicon Via (TSV) technologies enable high interconnect performance at relatively high fabrication cost compared to 3D packaging [2].

There are multiple approaches to manufacture TSVs. TSVs can be formed from the frontside using via-first, via-middle, or via-last processes. In addition, TSVs can be formed using a via-last process from the backside 22, 23. Major process steps for the TSV fabrication consist of TSV drilling, TSV insulation, TSV metallization, FEOL (front end of line) formation, BEOL (back end of line) formation, handler attachment, wafer thinning, and backside process. [24, 25] summarized the comparison of process flow for the three integration technologies. For the via-first process, the TSV formation (including TSV drilling, TSV insulation, and TSV metallization) is done before the forming of active devices. For the via-last process, on the contrary, the TSV formation is done after the formation of active devices, handler attachment, and wafer thinning. For the via-middle process, the TSV formation is completed across two phases. That is, the TSV metallization step of TSV formation is performed after the FEOL formation.

RESEARCH METHODS

To construct the analytic framework for deriving factors for evaluating and selection of the 3D IC TSV techniques, this research reviewed the related research works of semiconductor 3D package and literature being related to factors for technology assessment. Next, the DEMATEL method is employed to establish the causal relationships. Finally, the DNP will be applied to derive the influence weights based on the experts' perspectives. In summary, the assessment model consists of four main steps: (1) deriving the requirement by literature review; (2) structuring the causal relationship based on lead users' opinion by applying DEMATEL; and (3) evaluating the weights versus each criterion by using the DNP.

The DNP, the DEMATEL technique combining with ANP, was proposed by Tzeng [24, 26]. Combing the DEMATEL and ANP method, which had been review in this Section, the steps of this method can be summarized as follows:

Step 1: Calculate the direct-influence matrix by scores. Based on experts' opinions, evaluations are made of the relationships among elements (or variables/ attributes) of mutual influence using a scale ranging from 1 to 5, with scores representing "no influence" (1), "low influence" (2), "medium influence" (3), "high influence" (4), and "very high influence" (5). They are asked to indicate the direct effect they believe a factor will have on factor , as indicated by *dij* . The matrix ***D*** of direct relations can be obtained.

Step 2: Normalize the direct-influence matrix based on the direct-influence matrix ***D*** , the normalized direct relation matrix ***N*** is acquired by

$$\boldsymbol{N} = v\boldsymbol{D}; v = \min\{1/\max_i \sum_{j=1}^{n} d_{ij}, 1/\max_j \sum_{i=1}^{n} d_{ij}\}, i, j \in \{1, 2, ..., n$$

Step 3: Attaining the total-influence matrix ***T***. Once the normalized direct-influence matrix N is obtained, the total-influence matrix T of NRM can be obtained by

$$\boldsymbol{T} = \boldsymbol{N} + \boldsymbol{N}^2 + ... + \boldsymbol{N}^k = \boldsymbol{N}(\boldsymbol{I} - \boldsymbol{N})^{-1}.$$

where $\boldsymbol{T}$ is the total influence-related matrix; $\boldsymbol{N}$ is a direct influence matrix and $\boldsymbol{N} = [x_{ij}]_{n \times n}$; $\lim_{k \to \infty}(\boldsymbol{N}^2 + \cdots + \boldsymbol{N}^k)$ stands for an indirect influence matrix and $0 \leq \sum_{j=1}^{n} x_{ij} < 1$ or $0 \leq \sum_{i=1}^{n} x_{ij} < 1$, and only one $\sum_{j=1}^{n} x_{ij}$ or $\sum_{i=1}^{n} x_{ij}$ equal to 1 for $\forall i, j$. So $\lim_{k \to \infty} N^k = [\mathbf{0}]_{n \times n}$

The $(,)ij$ element .. of matrix denotes the direct and indirect influences of factor I on factor j.

Step 4: Analyze the result. In this stage, the row and column sums are separately denoted as $\boldsymbol{r}$ and $\boldsymbol{c}$ within the total-relation matrix $\boldsymbol{T}$

through following Equations.

$$T = [t_{ij}], \quad i, j \in \{1, 2, ..., n\},$$

$$r = [r_i]_{n\times1} = \left[\sum_{j=1}^{n} t_{ij}\right]_{n\times1},$$

$$c = [c_j]_{1\times n} = \left[\sum_{i=1}^{n} t_{ij}\right]_{1\times n},$$

where the r and c vectors denote the sums of the rows and columns, respectively.

Suppose r_i denotes the row sum of the ith row of matrix T. Then, r_i is the sum of the influences dispatching from factor i to the other factors, both directly and indirectly. Suppose that cJ denotes the column sum of the jth column of matrix . Then, is the sum of the influences that factor i is receiving from the other factors. Furthermore, when $i=j$ (i.e., the sum of the row sum and the column sum) represents the index representing the strength of the influence, both dispatching and receiving), is the degree of the central role that factor plays in the problem. If is positive, then factor primarily is dispatching influence upon the strength of other factors; and if $(r_i - c_i)$ is negative, then factor primarily is receiving influence from other factors [27, 28]. Therefore, a causal graph can be achieved by mapping the dataset of $(r_i + s_i, r_i - s_i)$ providing a valuable approach for decision making (see Chiu et al. [24]).

Now we call the total-influence matrix $T_C = [t_{ij}]_{n\times n}$ obtained by criteria and $T_D = [t_{ij}^D]_{n\times n}$ obtained by dimensions (clusters) from T_C. Then we normalize the ANP weights of dimensions (clusters) by using influence matrix . T_D

$$T_D = \begin{bmatrix} t_{11}^{D_{11}} & \cdots & t_{1j}^{D_{1j}} & \cdots & t_{1m}^{D_{1m}} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ t_{i1}^{D_{i1}} & \cdots & t_{ij}^{D_{ij}} & \cdots & t_{im}^{D_{im}} \\ \vdots & \vdots & & \vdots & \vdots \\ t_{m1}^{D_{m1}} & \cdots & t_{mj}^{D_{mj}} & \cdots & t_{mm}^{D_{mm}} \end{bmatrix} \begin{matrix} \longrightarrow d_1 = \sum_{j=1}^{m} t_{1j}^{D_{1j}} \\ \\ \longrightarrow d_i = \sum_{j=1}^{m} t_{ij}^{D_{ij}}, \\ \\ \longrightarrow d_m = \sum_{j=1}^{m} t_{mj}^{D_{mj}} \end{matrix}$$

$$d_i = \sum_{j=1}^{m} t_{ij}^{D_{ij}}, i = 1, ..., m, \; t_{ij}^{D} = 0.$$

Step 5: The original supermatrix of eigenvectors is obtained from the total-influence matrix $T = [t_{ij}]$. For example, D values of the clusters in matrix T_D, as Equation (8). Where if $t_{ij} < D$, then else $t_{ij}^D = t_{ij}$, and t_{ij} is in the total-influence matrix T. The total-influence matrix T_D needs to be normalized by dividing by the following formula. There, we could normalize the total-influence matrix and represent it as T_D.

$$T_D = \begin{bmatrix} t_{11}^{D_{11}}/d_1 & \cdots & t_{1j}^{D_{1j}}/d_1 & \cdots & t_{1m}^{D_{1m}}/d_1 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ t_{i1}^{D_{i1}}/d_i & \cdots & t_{ij}^{D_{ij}}/d_i & \cdots & t_{im}^{D_{im}}/d_i \\ \vdots & \vdots & & \vdots & \vdots \\ t_{m1}^{D_{m1}}/d_m & \cdots & t_{mj}^{D_{mj}}/d_m & \cdots & t_{mm}^{D_{mm}}/d_m \end{bmatrix}$$

$$= \begin{bmatrix} \alpha_{11}^{D_{11}} & \cdots & \alpha_{1j}^{D_{1j}} & \cdots & \alpha_{1m}^{D_{1m}} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \alpha_{i1}^{D_{i1}} & \cdots & \alpha_{ij}^{D_{ij}} & \cdots & \alpha_{im}^{D_{im}} \\ \vdots & \vdots & & \vdots & \vdots \\ \alpha_{m1}^{D_{m1}} & \cdots & \alpha_{mj}^{D_{mj}} & \cdots & \alpha_{mm}^{D_{mm}} \end{bmatrix}$$

where $\alpha_{ij}^{D_{ij}} = t_{ij}^{D_{ij}} / d_i$ This research adopts the normalized total-influence matrix T_D (here after abbreviated to "the normalized matrix") and the unweighted supermatrix W using Equation (9) shows theses influence level values as the basis of the normalization for determining the weighted supermatrix.

$$W^* = \begin{bmatrix} \alpha_{11}^{D_{11}} \times W_{11} & \alpha_{21}^{D_{21}} \times W_{12} & \cdots & \cdots & \alpha_{m1}^{D_{m1}} \times W_{1m} \\ \alpha_{12}^{D_{12}} \times W_{21} & \alpha_{22}^{D_{22}} \times W_{22} & \cdots & \cdots & \vdots \\ \vdots & \cdots & \alpha_{ji}^{D_{ji}} \times W_{ij} & \cdots & \alpha_{mi}^{D_{mi}} \times W_{im} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ \alpha_{1m}^{D_{1m}} \times W_{m1} & \alpha_{2m}^{D_{2m}} \times W_{m2} & \cdots & \cdots & \alpha_{mm}^{D_{mm}} \times W_{mm} \end{bmatrix}$$

Step 6: Limit the weighted supermatrix by raising it to a sufficiently large power by $\lim_{k\to\infty}(W^*)^k$ until the supermatrix has converged and become a long-term stable supermatrix to get the global priority vectors or called ANP weights.

EMPIRICAL STUDY RESULTS

In this article, the authors summarized the three dimensions and 20 criteria of emerging semiconductor 3D IC TSV TA based on the literature review and expert interviews using Delphi. The assessment dimension and criteria of 3D IC TSV selection are presented in Table 1. Three 3D IC TSV technology fields – via-first, via-middle, and via-last – were selected as the alternatives to be applied to the TA model. Based on the DEMATEL method, the total relationship matrices can be derived (refer TABLEs 2-5). The Influence Relationships Map (IRM) can further be constructed accordingly (refer Fig. 1 (a)-(d)). The weight versus each criterion can be calculated by using the DNP (refer TABLE 6).

The contributions of this research can be discussed in two respects – its advancement of TA methods and its assessment of 3D IC TSV techniques for future semiconductor 3D package technology. First, a novel TA framework was proposed and verified within a DEMATEL-based novel MCDM method with the ANP for the evaluation and selection of 3D IC TSV techniques. Compared to most decision-theory-based technology evaluation methods, the proposed method is significantly more reasonable. Very few scholars have tried to evaluate 3D IC TSV techniques for semiconductor 3D package technologies.

An examination of weights shown in TABLE 6 reveals that "business benefits" is the most important dimension, followed by "risk" and "technology superiority". Therefore, "business benefits" regarding company operation and the business model represents the core competence of 3D IC TSV manufacturers for sustaining their competitive edge. Profitability, market share and cost are the three most important factors. Moreover, although "business benefits" is the most important dimension, according to Figure 1, a good business model is based on technology superiority.

Based on this TA framework, the via-middle of 3D IC TSV technique was chosen as the best solution (refer TABLE 7) in the current situation of the semiconductor industry. At the same time, of the 20 assessment criteria, "partner risk", "long-term strategic relationship", and "heterogeneous integration" are the top three most significant factors. In the future, the proposed TA framework can be applied to the selection of other emerging technologies.

TABLE - 1 DIMENSION AND CRITERIA OF 3D IC TSV TECHNOLOGY ASSESSMENT

Aspects	Criteria	Definitions
Technology Superiority (D_1)	Technology quality (c_{11})	The term quality is an important term in business, but it is used with at least four meanings: 1) Performance quality —the quality of how well a product technically performs in its central function, a high - tech product of superior performance; 2) Design quality— the quality of a product design as focused on a particular application, a high - tech product focus on application; 3) Production quality— the quality of a production process that reproduces quantities of a product rapidly, without defects, and at low cost, a high - tech production process; 4) Service quality— the quality of a product in service as to durability and maintenance, a high - tech serviceable product [29].
	Technology reliability (c_{12})	Reliability provides the theoretical and practical means whereby the capability of devices performing their required functions for desired periods of time without failure can be expressed [30].

	Technology flexibility (c_{13})	Flexibility for the integration of die from different semiconductor technology nodes [31].
	Technology repeatability (c_{14})	Static repeatability is the standard deviation of repeated measurements made on the same object under identical conditions over a very short period of time (typically seconds or minutes). Dynamic repeatability is the standard deviation of measurements obtained from cycling the wafer into and out of the ellipsometer. Measurements arc performed over a short period of time (typically tens of minutes) by loading and unloading the wafer 30 times [32].
	Technology application (c^{15})	The drivers for through-silicon via (TSV) adoption can be divided into two major application areas. The first is products driven by form factor requirements. In some cases, this is also coupled with performance advantages. The second is high-performance computing, where the adoption of 3D TSV technology promises higher clock rates, lower power dissipation, and higher integration density. The technology will be adopted in many high-performance computing applications because it solves issues related to electrical performance, memory latency, power, and noise on and off the chip[33].
	Technology positioning (c_{16})	The end product of strategic technology management should be the identification, take-up and maintenance of an institutional position in relation to technology invention, innovation and improvement[34].
	Thermal Cooling Technique (c_{17})	Cooling and related thermal problems are the principal challenges facing 3D integrated circuits (3D-ICs). Active cooling techniques such as integrated inter-tier liquid cooling are promising alternatives for traditional fan-based cooling, which is insufficient for 3D-ICs. In this regard, fast full-chip transient thermal modeling and simulation techniques are required to design efficient and cost-effective cooling solutions for optimal performance, cost and reliability of packages and 3D ICs [35].
	3DEDA Capability (c_{18})	The design automation capability for 3D chip stacks. The capability is complex and not all challenges are fully solved yet, though more and more sophisticated EDA solutions are being proposed [36].
	Heterogeneous integration (c_{19})	3D integration of components with significant different device technologies as e.g. CMOS and MEMS [36].
	3D IC Test Capability (c_{110})	The migration to 3D-ICs connected by TSVs presents three new test challenges to the industry: 1) Managing the escape rate of defective die at wafer test to meet target post-packaging yield. 2) Testing memory die stacked on logic die configurations. 3)Testing logic stacked on logic die configurations. The 3D IC test capabilities include the industry-leading solutions for ATPG, compression, logic BIST, memory BIST, boundary scan, mixed-signal BIST and silicon learning [36].
Business benefits (D_2)	Cost (c_{21})	The cost of each 3D IC manufacturing activity is calculated by analyzing every potential cost contributor for every step—time, labor, material cost, tooling cost, equipment cost (including depreciation), and yield loss[37].
	Market share (c_{22})	Market share is the proportion or percentage of the total market that is controlled by either a single business or a particular product or service. It too can be measured either in terms of volume or value. However, most of the time it is measured in terms of the total percentage of that market or by value alone [38].
	Profitability (c_{23})	Profit-ability is the ability of a business to generate profits and it is an ongoing state of being, a steady state whereas profits are discrete events in time [39].
	Long term strategic relationship (c_{24})	Social capital refers to a firm's relationships with other companies that have important resources; effective social capital is a product of relationships that have developed through long-term interactions between firms [40].
	Diffusion time (c_{25})	Diffusion is "the process by which an innovation is communicated through certain channels over time among the members of a social system" [41].
Risks (D_3)	Integration yield risk (c_{31})	Extra manufacturing step of 3D TSV adds risks for defects and yield losses [42].
	Technological risk (c_{32})	There are two classes of risk in any engineering project: (a) that the project will fail to deliver its objectives on time, within budgeted costs, or at all; and (b) that the delivered product or service will behave in undesired ways, causing problems, injury or damage [43]. The study of technology risk involves the analysis of how technology exposes society to different threats or hazards [43].
	Commercial risk (c_{33})	Most of the money a business may lose upon the commercial failure of a new product or new service occurs here in the commercialization stage, when the new product fails to deliver a performance or price advantage to a customer against competitive products; this is the commercial risk in innovation [44]. The downside of introducing new technology is the increase in commercial risk [45]. The balancing of risk against technical advantage is a fundamental challenge that must be accepted by the chip designers.
	Risks of partnership (c_{34})	The risks of partnering include the increasing of project complexity, loss of autonomy and control, loss of trade secrets, dilution of competitive advantage, legal issues and antitrust concerns [46].
	Capex risk (c_{35})	Capex risk is the risk being associated with capital expenditure [47].

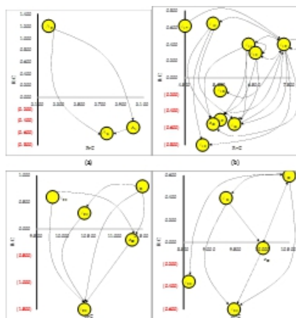

Figure 1: The IRM of (a) dimensions and criteria in dimension (b) D_1, (c) D_2, and (d) D_3

TABLE-2 TOTAL RELATION MATRIX $T_{Dimension}$ OF CRITERIA.

	D_1	0.728	1.368	1.224
Tdimensions=	D^2	0.792	0.752	0.936
	D_3	0.648	0.888	0.584

TABLE-3 TOTAL RELATION MATRIX OF CRITERIA

Td_1 =	*c11*	0.263	0.342	0.326	0.303	0.376	0.387	0.242	0.338	0.407	0.336
	c12	0.284	0.195	0.263	0.230	0.291	0.300	0.177	0.258	0.276	0.256
	c21	0.203	0.219	0.159	0.157	0.209	0.216	0.130	0.239	0.267	0.218
	c22	0.329	0.303	0.350	0.202	0.317	0.348	0.207	0.343	0.388	0.320
	c23	0.344	0.358	0.322	0.298	0.267	0.382	0.258	0.334	0.383	0.332

	c24	0.304	0.301	0.281	0.248	0.311	0.236	0.193	0.256	0.355	0.275
	c25	0.289	0.286	0.265	0.194	0.296	0.264	0.139	0.261	0.337	0.240
	c26	0.252	0.209	0.273	0.221	0.258	0.287	0.150	0.183	0.304	0.247
	c31	0.402	0.396	0.380	0.349	0.411	0.423	0.303	0.372	0.343	0.388
	c32	0.278	0.275	0.318	0.223	0.305	0.315	0.168	0.272	0.351	0.206

TABLE-4 TOTAL RELATION MATRIX T_{D2} OF CRITERIA

	c11	1.059	1.335	1.394	1.177	1.145
	c25	1.145	1.043	1.285	1.086	0.982
***T** D2=*	*c26*	0.951	0.977	0.853	0.867	0.777
	c31	1.110	1.229	1.175	0.875	0.956
	c32	1.057	1.212	1.197	1.003	0.796

TABLE-5 TOTAL RELATION MATRIX T_{D3} OF CRITERIA

	c11	0.765	1.079	1.067	1.033	0.883
	c25	0.993	0.907	1.062	1.108	0.955
***T** D3 =*	*c26*	1.048	1.254	1.007	1.217	1.096
	c31	0.820	0.967	1.002	0.810	0.874
	c32	0.805	0.857	0.897	0.900	0.654

TABLE-6 WEIGHTS OF 3D IC TSV TECHNOLOGY ASSESSMENT

Aspects	Criteria	Weight	Ranking
Technology Superiority (D_1)	Technology quality (c_{11})	2.97%	14
	Technology reliability (c_{12})	2.89%	16
	Technology flexibility (c_{13})	2.94%	15
	Technology repeatability (c_{14})	2.45%	19
	Technology application (c_{15})	3.06%	13
	Technology positioning (c_{16})	3.17%	12
	Thermal Cooling Technique (c_{17})	1.97%	20
	3D EDA Capability (c_{18})	2.87%	17
	Heterogeneous integration (c_{19})	3.45%	11
	3D IC Test Capability (c_{110})	2.84%	18
Business benefits (D_2)	Cost (c_{21})	7.51%	3
	Market share (c_{22})	8.10%	2
	Profitability (c_{23})	8.20%	1
	Long term strategic relationship (c_{24})	7.04%	7
	Diffusion time (c_{25})	6.53%	8
Risks (D_3)	Integration yield risk (c_{31})	6.28%	10
	Technological risk (c_{32})	7.15%	5
	Commercial risk (c_{33})	7.16%	4
	Risks of partnership (c_{34})	7.14%	6
	Capex risk (c_{35})	6.30%	9

TABLE-7 PERFORMANCE SCORES OF 3D IC TSV SOLUTIONS

Aspects	Criteria	Via First	Via Middle	Via Last
Technology Superiority (D_1)	Technology quality (c_{11})	0.519	0.519	0.519
	Technology reliability (c_{12})	0.404	0.505	0.505
	Technology flexibility (c_{13})	0.308	0.513	0.410
	Technology repeatability (c_{14})	0.343	0.343	0.343
	Technology application (c_{15})	0.321	0.536	0.428
	Technology positioning (c_{16})	0.554	0.443	0.443
	Thermal Cooling Technique (c_{17})	0.207	0.345	0.276
	3D EDA Capability (c_{18})	0.501	0.301	0.200
	Heterogeneous integration (c_{19})	0.120	0.602	0.361
	3D IC Test Capability (c_{110})	0.199	0.397	0.397
Business benefits (D_2)	Cost (c_{21})	0.804	1.005	1.005
	Market share (c_{22})	1.083	0.867	0.650
	Profitability (c_{23})	0.878	0.658	0.878
	Long term strategic relationship (c_{24})	0.377	0.941	0.565
	Diffusion time (c_{25})	0.524	0.699	0.874
Risks (D_3)	Integration yield risk (c_{31})	0.739	0.923	0.923
	Technological risk (c_{32})	1.050	0.840	0.840
	Commercial risk (c_{33})	0.841	1.051	1.051
	Risks of partnership (c_{34})	0.420	1.049	0.630
	Capex risk (c_{35})	0.926	0.926	0.741

CONCLUSIONS

Three-dimensional packaging is one of the main MCP techniques that emerged in recent years. The 3D integrated circuits with TSV techniques can achieve smaller chip area with lower power consumption than other MCP solutions. Very few researchers have studied the evaluation and selection of 3D IC TSV techniques, despite their importance. A DEMATEL-based novel MCDM method with the ANP was proposed in this paper. Based on expert opinions, via-middle should be the most suitable solution for future 3D IC TSV techniques. The results of this empirical study can serve as a basis for future semiconductor 3D package technology development.

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