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DESIGN AND IMPLEMENTATION OF ALU USING APPLICATION SPECIFIC REVERSIBILITY WITH VEDIC MATHEMATICS

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ABSTRACT The Main Objective of the Project is to Design Vedic Mathematics based "ALU" using Reversibility Technique for DSP Applications. In Order to Reduce Delay, Area, Complexity, power consumption, Improve the High speed. The Proposed "ALU" is Coded in Verilog, Synthesized and Simulated using Xilinx ISE Tool. Reversibility is used to reduce area, complexity. And the multiplication is done by using Vedic Multiplier; Vedic multiplier is used to increase the speed. We are Designing our Architecture in Verilog HDL code and also simulated using Vivado 2015.2 Tool and Hardware Implementation on ZYNQ Board(FPGA).The Project functionality input and output to the system is digital data. And the process expected to be done in the system is Arithmetic and logical operations and Multiplication process. The specifications of "ALU" are two 4bits digital data input bit size and 8bit digital data output bit size.

KEYWORDS : ALU, Reversibility, Reversible logic gates, Vedic Mathematics, Urdhva Triyambakam Sutra.

1.INTRODUCTION

"ALU" Stands for Arithmetic Logic Unit. ALU is the major driving component of a processor. Arithmetic Logic Unit is a digital circuit that performs Arithmetic (Add, Sub, Mult, Inc, Dec, etc) and Logical (And, or, nor, etc) Operations.

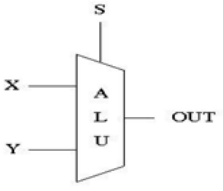


Figure1: Block diagram of ALU

Now a day's all CPU units, any machinery parts utilizes a basic arithmetic operations like addition, subtraction, multiplications. "ALU "plays a vital role in CPU's, Microprocessors, and Microcontrollers so ALU is the heart of the processor. The central processing unit speed is greatly depends upon the ALU so we need to have fast and efficient ALU. In this ALU all the modules (Adder, Sub tractor, Multiplier, Logical, and Mux) are designed by using reversible logic gates. Here Vedic algorithm (Urdhva Triyambakam Sutra-16 sutras) was used for the faster execution of an arithmetic module of an ALU. Here Vedic Multiplier is designed using Reversible logic gates and adders. Vedic multiplier increases the speed of the Architecture. Here Reversibility is used to reduce the complexity. Reversible gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between inputs and outputs.

II.REVERSIBLE TECHNIQUE

The Reversible logic gate must be run forward and backward. i.e.; the input can also be recovered or retrieved from the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. This generates a unique output vector for each input vector. This prevents the loss of information which causes power dissipation. Reversibility is used to reduce the complexity. It requires the input and output pin count to be same. Also each input state must correspond to a particular unique state of the output.i.e. Output states cannot be shared by more than one input states available.

GOALS OF REVERSIBLE LOGIC

- Minimize the delay.
- Minimize the total no of gates.
- Minimize the garbage.
- Minimize the width of the circuit.

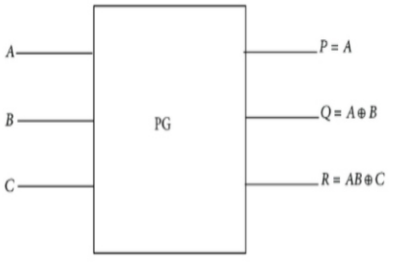
A Gate with N inputs and N outputs is called N*N gate. Where N= {1, 2, 3, 4----------}.

Examples Like: Peres gate, HNG gate, BJN gate, TSG gate, Feynman gate/CNOT gate are Reversible Logic Gates.

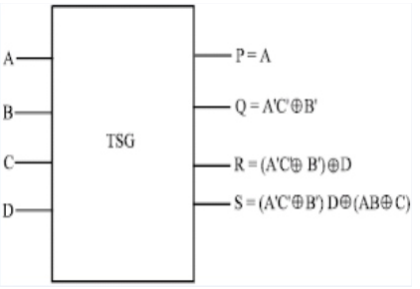
A. REVERSIBLE GATES

The Following are the reversible logic gates used in this paper.

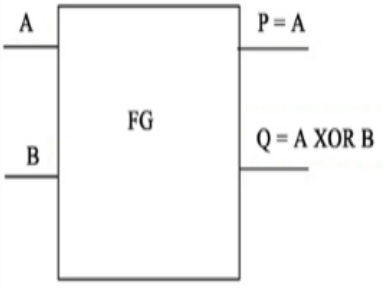
PERES GATE



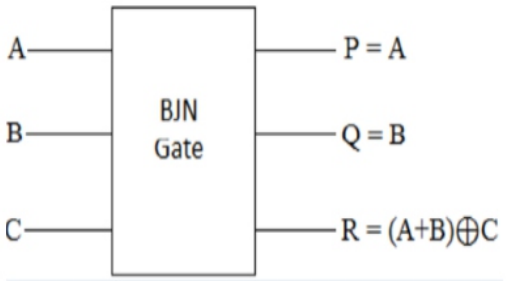
TSG GATE



FEYNMAN GATE



BJN GATE



HNG GATE

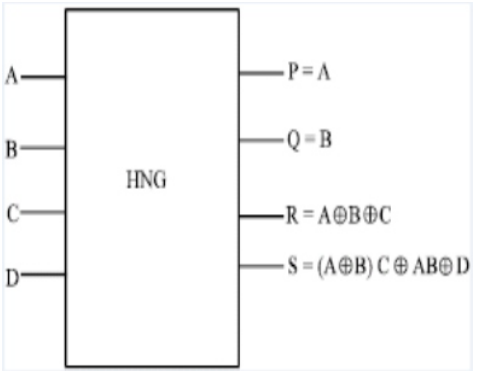


Figure2: Reversible logic gates

Importance of reversible gates

- Peres gate is a 3x3 gate. Its quantum cost is 4.It is used for half adder purpose. To act like half adder put c=0.
- TSG gate is a 4x4 gate. Its quantum cost is 14. It is used for the rest of the Logical operations based on the control signals. To select the logical operation c&d pins are used as control signals.
- Feynman gate is a 2x2 gate. Its quantum cost is 1.It is also called as CNOT gate.
- BJN gate is a 3x3 gate. Its quantum cost is 5.It is used for only OR and NOR operations. To act like Logical operation put c=0 & c=1.
- HNG gate is a 4x4 gate. Its quantum cost is 6.It is used for full adder purpose. To act like full adder assign d=0. & c=carry bit.

III. DESIGN OF ALU

The proposed "ALU" performs total 13 operations. i.e.; 5 arithmetic operations and 8 logical operations. The operations performed based on the control signal. "ALU" design uses reversible logic gates. The specifications of "ALU" are 4bit control signal and two 4bits input digital data and 8bit output digital data.

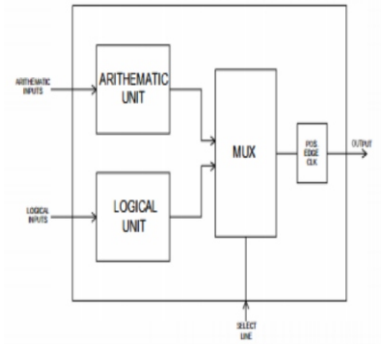


Figure3: Proposed ALU Architecture

Therefore the different Arithmetic & Logical Operations are performed based on the different control signal is shown in the below table.

Table1.Operations Table

Control Signal	Operation
0000	Addition
0001	Subtraction
0010	Multiplication
0011	Increment
0100	Decrement
0101	A.B
0110	A⊕B
0111	$\overline{A \oplus B}$
1000	$\overline{B}$
1001	$\overline{A.B}$
1010	$\overline{A}.B$
1011	A+B
1100	$\overline{A+B}$

A. 4-Bit Full Adder/Subtractor

Reversible full adder/subtractor is designed by using 4 HNG gates. This adder is a ripple carry adder. Here HNG gate is used because it acts like full adder application when c, d pins of HNG gate is said to 0.When s=0, the circuit acts like 4-bit full adder. When s=1, the circuit acts like subtractor. A control signal S is used to switch between subtractor and adder mode.

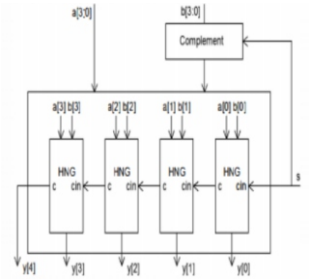


Figure4: 4-BitReversible Full Adder/Subtractor

B. 4-bit Reversible Vedic Multiplier

This Reversible Vedic Multiplier requires four 2-bit multipliers and 3 adders. Here Multiplication is based on the Urdhva Triyambakam Sutra. This Technique uses less no of computational steps to get the result. And this multiplication technique is faster compare to conventional multipliers. The four bit inputs are split into two parts of 2bit each. Each part of input is multiplied with each part of the other input using the four 2-bit multipliers. The last two bits of product of a[1:0] and b[1:0] is assigned to output q[1:0].The first two bits are added to the product of a[1:0] and b[3:2].The product of a[3:2] and b[1:0] is added by the left shifted by 2-bit product of a[3:2] and b[3:2].The result of these two addition is added to get output bits q[7:2]. Area is reduced compare to previous multiplier.

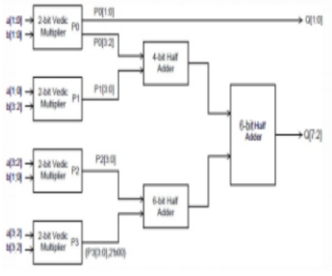


Figure5: 4-Bit Reversible Vedic multiplier

C. Logical Unit

This 4-bit Logical Unit performs the 8 logical operations (AND, NOR, XNOR, XOR, NOT, NAND, A'B, OR, NOR) on two 4-bit numbers. Thus overall logic unit uses only two types of reversible logic gates (BJN, TSG) to implement 8 logic operations so as to reduce the complexity and power.

D. Multiplexer

A Multiplexer is a digital circuit that has multiple inputs and a single output. The selection of one of the n inputs is done by the select inputs. It has one output selected at a time. It is also known as data selector. Multiplexer means many into one. The select lines determine which input is connected to the output.

IV TEST RESULTS

A.Simulation Results

The ALU is coded in Verilog and Simulated using Vivado Tool.

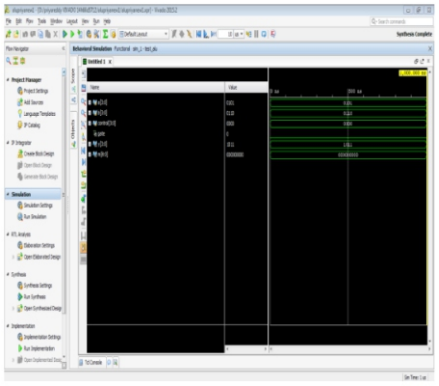


Figure6: Simulation result of ALU

Interpretation: In the above simulation, when control signal =0000, then addition operation is performed. For different control signals different operations are performed as shown in the operations table. Here in this simulation when inputs a=0101, b=0110 then output is y=1011.

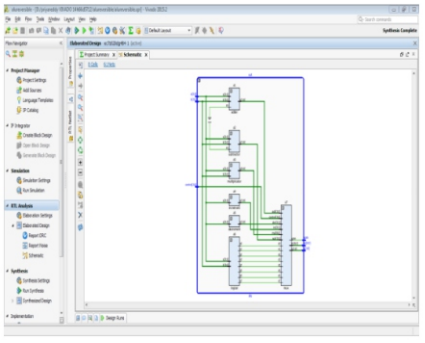


Figure7: RTL Schematic view of ALU

B. Hardware Implementation Results

ZYNQ Board (FPGA) 7000 series was implemented in family XC7Z020 with package number CLG484 and speed grade is -1.Vendor is Xilinx.

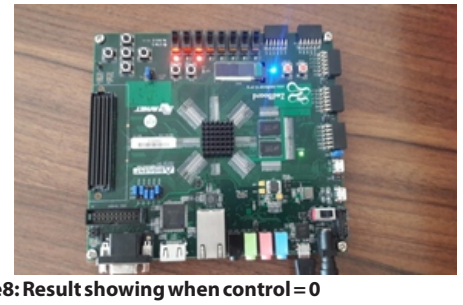


Figure8: Result showing when control = 0

Interpretation: When inputs a=0010, b=0011 then output is y=0101.If control is 0 then addition operation is performed.

V.RESULT ANALYSIS

The Following are Proposed ALU results compared with previous ALU results.

Table2: Comparision Table

Parameter	Achieved in reference paper/ any available standard	As per project objective	As per test report
Delay	14.3ns	11ns	6.14ns
Speed	less	more	more
Number of slices (Area)	40	-	37
Complexity	more	less	less

The result shows that better performance in proposed ALU in various aspects like delay, speed, complexity, area. Therefore the proposed ALU shows the better results compared to conventional ALU.

Advantages

- Delay Reduces.
- Complexity Reduces.
- High Speed.
- Area and Power Reduces.

Applications

- Digital signal processing (DSP).
- Microprocessors.
- Nanotechnology.
- Optical computing and Quantum computer.

VI CONCLUSION

The proposed ALU has been designed by using reversible logic gates for DSP application. And simulated in Vivado tool and Implemented on Zynq board. Reduction in delay, complexity, area has been achieved. And improves the speed.

Future Scope

Future work includes using the reversibility for designing ALU with High speed radix 4 booth multiplier gives better performance in various aspects like delay, speed and power.

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