



## FPGA BASED IMPLEMENTATION OF ROBUST ROUTER ARCHITECTURE

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### ABSTRACT

The router is a "Robust Router" consist of one input port from which the packet enters. It has three output ports where the packet is driven out. Packet contains three parts. They are Header, and data and frame check sequence. Packet width is of 8 bits and length of the packet transferring can be between 1 to 63 bytes. The switch drives the packet to respective ports based on this destination address of the packet. Each output has 8 bit unique port address. If the destination address of the packet matches the port address, then the switch drives the packet to the output port, length of the data is of 8 bits. In this proposed paper the Xilinx Vivado IDE Tool is used for synthesis and is used for simulation. In the proposed design the FSM is designed with reduced number of states, due to reduction of states the amount of time to produce the response became less obviously the frequency is improved. The Robust Router design is done by using of the 3 blocks, the blocks are 8-Bit Register, Router controller (FSM) and output block which is consists of 3 FIFO's combined together are store packet of data and when you want to data that time the data read from the FIFO's. In this router design has three outputs that is 8-Bit size and one 8-bit data port it using to drive the data into router we are using the global clock and reset signals, and the err signal and suspended data signals are output's of the router. The FSM controller gives the err and suspended\_data\_in signals and We are designing our architecture in Verilog HDL code using Vivado 14.3 and implemented on Zynq Board (FPGA).

**KEYWORDS** : Simulation Router, FIFO, FSM, Register blocks, Verilog

### INTRODUCTION

My research is based on this paper "**vlsi based robust router architecture**". Now in this paper I have designed a four port router which is advancement for the previous router network. we have ability to connect a network of four systems. I observed the results using Verilog HDL.

The challenge of the verifying a large design is growing exponentially. There is a need to define new methods that makes functional verification easy. several strategies in the recent years have been proposed to achieve good functional verification with less effort. Recent advancement towards this goal is methodologies. The open verification methodologies is built on system Verilog and used effectively to achieve maintainability, reusability, speed of verification etc. This project is aimed at building a reusable test bench for verifying four port router by using system Verilog.

A router is the most important component in a NOC. It is the communication backbone of a NOC system. So it should be designed for maximum efficiency and throughput. A router is used in a network for directing the traffic from source to destination. It coordinates the data flow which is very crucial in communication networks. The architecture of a router consists of an input port, an output port, a switching matrix to connect the input port to the output port, and a local port that connects the router to the corresponding IP core. Routers are intelligent devices that receive incoming data packets, inspect their destination and figure out the best path for the data to move from source to destination. A router's architecture determines its critical path delay which affects per hop delay and network latency. So the design of the router should be such that it meets the required latency and throughput requirements amidst tight area and power constraints. The design efficiency of the router determines the performance of the network. A router decodes the information provided by the incoming message based on the routing function and destination of the message. A router is built according to the OSI model of NOC.

### DESCRIPTION

The router has a one input port from which the packet enters. It has three output ports where the packet is motivated out. Packet contains 3 parts. They are present direction and frame check chain Packet width is 8 bit and length of the pot can be sandwiched between 1 byte to 63 bytes. Packet header contains three fields DA and length goal (DA) of the envelope is of 8-bits. The switch drives the packet to respective ports based on the destination tackle of the packets.

Each output port has a unique port address. If the destination address of the packet matches the port address, then the switch drives the packet to the output port, length of the data is of 8 bits and from 0 to 63 bytes. The register has a positive edge clock, an active high clock enable and an active high asynchronous reset. The output of the register is the input to the de-multiplexer. The data input to the register is transfer to the output port at the positive edge of the clock if and only if the enable is 1, and reset is 0. If the reset is 1, then the output port of the register is set to zero. If enable is 0, then the output port keeps its current value. Since ROUTER is synchronous, it has a clock pulse along with the data. RS-232 and other asynchronous protocol do not use clock pulse, but the data must be timed very accurately. since ROUTER has a lock signal, the clock can vary without disrupting the data. The data rate will simply changes along with the changes in the clock rate. The ROUTER design is done by using of three blocks, they are 8-bit register, router controller is design by using FSM design and the output block consists of three FIFOs. FSM controller gives the err and suspended data in signals. This functions are discussed clearly.

This router supports three parallel connections the same time. It uses store and forward type of flow control and FSM controller deterministic routing which improves performance of router. The switching mechanism used here is packet switching which is generally used on chip. In the packet switching the data transfers in the form of packets between co-operating routers and independent decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels. The arbiter is of rotating priority scheme so that every channel once get chance to transfer its data. In the router both input and output buffering is used so that congestion can be avoided at both sides. The clock signal provided by the master to provide synchronization. The clock signal controls when data can change and when it is valid for reading. Since ROUTER has a clock signal, the clock can vary without disrupting the data. The data rate will simply change along with the changes in the clock rate. ROUTER is more suited for data stream application, communication between IP's.

### OPERATION

The Four Port Router Design is done by using of the three blocks. The blocks are 8-Bit Register, Router Controller and output block as shown in Fig 4.1. The router controller is design by using FSM design and the output block consists of three FIFO's combine to gather.

The FIFO's store data packets and when you want to send data that time the data will read from the FIFO's. In this router design has four outputs i.e. 8-Bit size and one 8-bit data port. It is used to drive the data into router. we are using the global clock, reset signals, error signal and suspended data signals are the output's of the router. The FSM controller gives the error and SUSPENDED\_DATA\_IN signals.

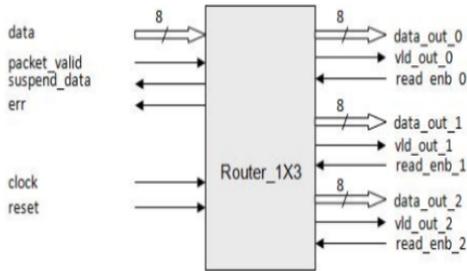


Fig: Block Diagram of Router

These functions are discussed clearly in below FSM description. The ROUTER can operate with a single master device and with one or more slave devices. If a single slave device is used, the RE (read enable) pin may be fixed to logic low if the slave permits it. Some slaves require the falling edge (HIGH LOW transition) of the slave select to initiate an action such as the mobile operators, which starts conversion on said transition. With multiple slave devices, an independent RE signal is required from the master for each slave device. There are 3 fifos used in the router design. Each fifo is of 8 bit width and 16 bit depth. The fifo works on system clock. It has synchronous input signal reset. If resetn is low then full is 0, empty is 1 and data out is 0. In the Write. operation, The data from input data in is sampled at rising edge of the clock when input write\_enb is high and fifo is not full. In the Read Operation, the data is read from output data out at rising edge of the clock, when read\_enb is high and fifo is not empty. Read and Write operation can be done simultaneously. Full indicates that all the locations inside fifo has been written. Empty indicates that all the locations of fifo are empty.

Data packet moves in to the input channel of one port of router by which it is forwarded to the output channel of other port. Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are present at all ports to store the data temporarily. The buffering method used here is store and forward. Control logic is present to make arbitration decisions. Thus communication is established between input and output ports.. According to the destination path of data packet, control bit lines of FSM are set. The movement of data from source to destination is called switching mechanism The packet switching mechanism is used here, in which the flit size is 8 bits .Thus the packet size varies from 0 bits to 8 bits. A detailed explanation of Design is as follow.

**Packet Format**

Packet contains 3 parts. They are Header, payload and parity. Packet width is 8 bits and the length of the packet can be between 0 bytes to 63 bytes.

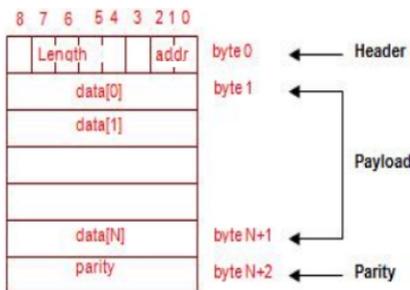


Figure. Packet format

The characteristics of the DUV input protocol are as follows:

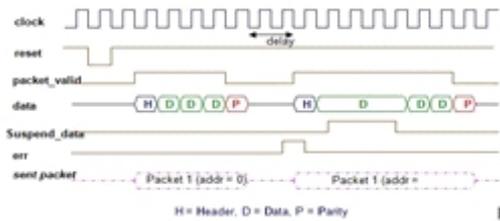


Figure Router Input Protocol

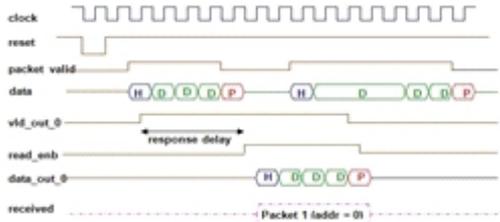


Figure Router output Protocol

**Router Architecture**

The Four port Router Design is done by using of the three blocks .the blocks are 8-Bit Register, Router controller and output block. the router controller is design by using FSM design and the output block consists of three fifo's combined together the fifo's are store packet of data and when u want to data that time the data read from the FIFO's. In this router design has three outputs that is 8-Bit size and one 8\_bit data port it using to drive the data into router we are using the global clock and reset signals, and the err signal and suspended data signals are output's of the router .the FSM controller gives the err and suspended\_data\_in signals .this functions are discussed clearly in below FSM description

The router\_reg module contains the status, data and parity registers for the Network router\_1x3.These registers are latched to new status or input data through the control signals provided by the fsm\_router.There are 3 fifo's output ports, which stores the data coming from input port based on the control signals provided by fsm\_router module. The fsm\_router block **provides** the control signals to the fifo, and router\_reg module.

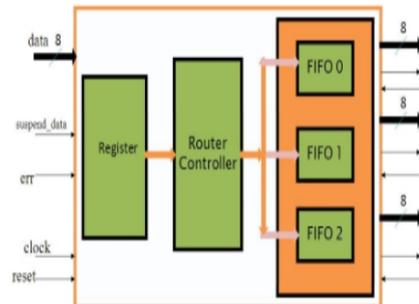


Figure Four Port Router Architecture

The Router blocks are Register Router controller(FSM), FIFO Output Block

**Router Output Block**

There are 3 fifos used in the router design. Each fifo is of 8 bit width and 16 bit depth. The fifo works on system clock. It has synchronous input signal reset. If reset is low then full =0, empty = 1 and data\_out= 0.The FIFO has doing 3 deferent operations

**Write operation:** The FIFO write operation is done by when the data from input data\_in is sampled at rising edge of the clock when input write\_enb is high and fifo is not full. in this condition only FIFO Write operation is done.

**Read Operation:** The FIFO Read Operation is The data is read from output data\_out at rising edge of the clock, when read\_enb is high and fifo is not empty.

Read and Write operation can be done simultaneously.

**Full:** it indicates that all the locations inside fifo has been written.

**Empty:** it indicates that all the locations of fifo are empty.

This module provides synchronization between fsm and fifo modules. It provides faithful communication between single input port and three output ports. It will detect the address of channel and will latch it till packet\_valid is asserted, address and write\_enb\_sel will be used for latching the incoming data into the fifo of that particular channel. A fifo\_full output signal is generated, when the present fifo is full, and fifo\_empty output signal is generated by the present fifo when it is empty. The output vld\_out signal is generated when empty of present fifo goes low, that means present fifo is ready to read. The write\_enb\_reg signal which comes from the fsm is used to generate write\_enb signal for the present fifo which is selected by present address. This module contains status, data and parity registers required by router. All the registers in this module are latched on rising edge of the clock. Data registers latches the data from data input based on state and status control signals, and this latched data is sent to the fifo for storage. Apart from it, data is also latched into the parity registers for parity calculation and it is compared with the parity byte of the packet. An error signal is generated if packet parity is not equal to the calculated parity. Internal parity register stores the parity calculated for packet data, when packet is transmitted fully, the internal calculated parity is compared with parity byte of the packet. An error signal is generated if packet parity is not equal to the calculated parity.

The „fsm\_router module is the controller circuit for the router as shown in Fig 4.10. This module generates all the control signals when new packet is sent to router. These control signals are used by other modules to send data at output, writing data into the fifo.

**FEATURES**

- Full duplex synchronous serial data
- Variable length of transfer word up to 64 bytes
- HEADER is the first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently
- 3 receivers select lines

- Fully static synchronous design with one clock domain
- Technology independent
- Fully synthesizable

In this project, the main aspect is designing a Robust Router by using verilog Code. The advantage of using verilog code is to generate physical layout directly after conventional digital synthesis and place-and-route as generating layout by using analog components is a time taking process. The three main components are Register, FSM and FIFO's.

We are designing our architecture in Verilog HDL code using Vivado 14.3 and implemented on Zynq Board .The below section will give brief introduction about Verilog HDL and Vivado Design Suite.

**SIMULATION RESULTS**

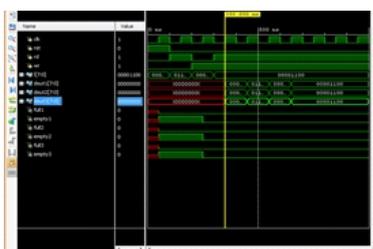


Figure simulation waveform

**Device Utilization Summary: XILINX Vivado IDE TOOL**

Resources	used	available	utilization
FF	45	106400	0.04%
LUT	41	53200	0.08%
Memory LUT	8	17400	0.05%
I/O	28	200	14%
BUFG	1	32	3.12%

**ADVANTAGES**

Due to reduction of states the amount of time to produce the response became less obviously the frequency is improved.

Less area requirement

At the same time the memory required to design of this Router chip is also reduced.

**APPLICATIONS**

These are widely used in the network on chip applications

- When multiple routers are used in interconnected networks, the routers exchange information about destination addresses, using a dynamic routing protocol.
- Each router builds up a table listing the preferred routes between any two systems on the interconnected networks.
- A router has interfaces for different physical types of network connections, (such as copper cables, fiber optic, or wireless transmission).
- These are widely used in the network on chip applications

**CONCLUSION**

In this paper, a reduced area(NO OF LUT'S) of a four port functionality is implemented in Verilog HDL and proven that this architecture consumes less resources in terms of no of LUT 'S ,slices and no of IO Buffers. In this paper the Xilinx Vivado IDE Tool is used for synthesis and for simulation. In future there is a chance to estimate the power consumption also. ROUTER was improved by reducing the usage of no of LUTs and memory utilize requirements by improving the frequency.

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