Original Research Paper Engineering

A TOPOLOGY FOR CASCADED MULTILEVEL INVERTER OF 31 LEVEL WITH REDUCED SWITCHES

B. Balaji CK College of Engineering & Technology Cuddalore, Tamil Nadu, India

ABSTRACT In this research work, a topology is formed of Voltage sources that are connected in series/parallel by the switching devices makes it easily extensible to higher number of output voltage levels associated with less number of switches, capacitors, gate driver circuits, protection circuits for switches and blocking voltage on switches. The size, complexity and power consumption in the gate driving circuits is also reduced. Reduction of rating of the switches is another advantage. The total harmonic distortion (THD) is reduced with more number of steps in output voltage without using pulse width modulation techniques. This topology is proposed to get high 31 levels. In the asymmetric topologies, the values of dc voltage sources magnitudes are unequal or changed dynamically. If the voltage sources are changed during the converter operation, the voltage balancing should be done for active power transfer. In this paper voltage balancing technique is analyzed for cascaded multilevel inverter which shows how to operate the converter in order to maintain equal charge/discharge rates from the dc sources and Simulation results for active power transfer & reactive power transfer are shown.

KEYWORDS : cascaded multilevel inverter, switches, total harmonic distortion.

INTRODUCTION

Numerous industrial applications have begun to require high power apparatus in recent years. Multilevel inverters have become more popular over the years in industrial propel applications and high power applications with the promise of less disturbances, smaller common-mode voltage, the possibility to function at lower switching frequencies, and good potential for further developme nts than ordinary two-level inverters. Though Conventio nal two-level inverters are effective, but create harmonic distortions in the output voltage, EMI and high dv/dt (compared to multilevel inverters). As a result the most attractive applications of multilevel inverters are in the medium to high voltage ranges. The concept of Multilevel Inverters does not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform with lower dv/dt and lower harmonic distortions. With more voltage levels in the inverter, the waveform becomes smoother, but with many levels the design becomes more complicated, with more components. A multilevel converter not only achieves high power rating, but also enables the use of renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application. Proposed topology has fewer switches than that of in symmetric topology.

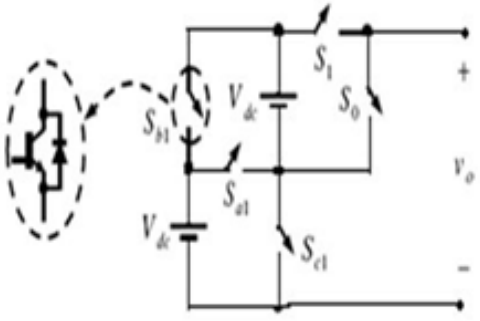
Several multilevel inverter topologies have been developed like flying capacitor, neutral point clamped, Cascaded H-bridge (CHB). Among these topologies, the cascaded H bridge inverter has received much attention.

The proposed topology is of cascaded multilevel inverter with asymmetrical configuration, since it uses several levels of dc voltage sources, which would be available from batteries, ultra capacitors, or fuel cells. Because of these several levels of dc sources may cause voltage unbalances which leads to the increase of harmonics and total harmonic distortion. Proposed topology shows how to operate this converter in order to maintain equal charge/discharge rates from the dc sources. This is called voltage balancing technique in the multilevel inverter. With this technique the harmonic content is also reduced. Since switching frequency is restricted by switching losses in high power and high voltage applications, multilevel inverters have found wide acceptance as they can achieve a low harmonic component with low switching frequency. Furthermore, low blocking voltage by switching devices is the other advantage of this type of converters as well as minimum harmonic distortion and switching losses.

The blocked voltage by each switch in a specific unit is same as the other switches used in the same unit and is equal to the magnitude of the dc voltage source used in the unit. Therefore, the number of gate driving circuits is reduced and as a result the size of multilevel inverter and its power consumption are reduced. Another feature of the proposed topology is that there is any kind of necessity to bidirectional switches. In this paper, a new procedure is recommended to find out the magnitude of the dc voltage sources and produce all output voltage levels. Finally, a method to find out the optimal number of switches and dc voltage sources so that have the maximum output voltage levels with the minimum blocked voltage by switches is presented.

PROPOSED SYSTEM

In this paper, the proposed multilevel inverter not only has the modularity feature of cascaded topologies but also consists of the ability of series and parallel connections of dc voltage sources. Series and parallel connections of the dc voltage sources increase the output voltage levels or given current to the multilevel inverter, respectively. In the proposed topology, the magnitude of the dc voltage sources differs from one unit to another.



Combination Of Switches		Confg. of DC Voltage Sours.
ON	OFF	
Sa1-San-1	Sb1-Sbn-1, Sc1-Scn-1	Series
Sb1-Sbn-1, Sc1-Scn-1	Sa1-San-1	Parallel
Current flow in Sb2-Sb-1, Sc2-Scn-1	Sa2-San-1, Sb1, Sc1	Series/Parallel

Figure 1: Proposed basic unit.

When the switches S0 and Sc1 become ON, the voltage level at the output is zero. By turning on the switches S1, Sb1, and Sc1, the two dc voltage sources are paralleled and Vdc is produced at the output. Similarly, when the switches S1 and Sa1 become ON, the two dc voltage sources could be connected in series and 2Vdc is produced at the output as shown in table 1.

TABLE - 1 SWITCHING FOR BASIC UNIT

SWITCHING STATES					Vo
Sa1	Sb1	Sc1	S1	S0	
0	0	1	0	1	0
0	1	1	1	0	Vdc
1	0	0	1	0	2Vdc

PRINCIPLE OF OPERATION

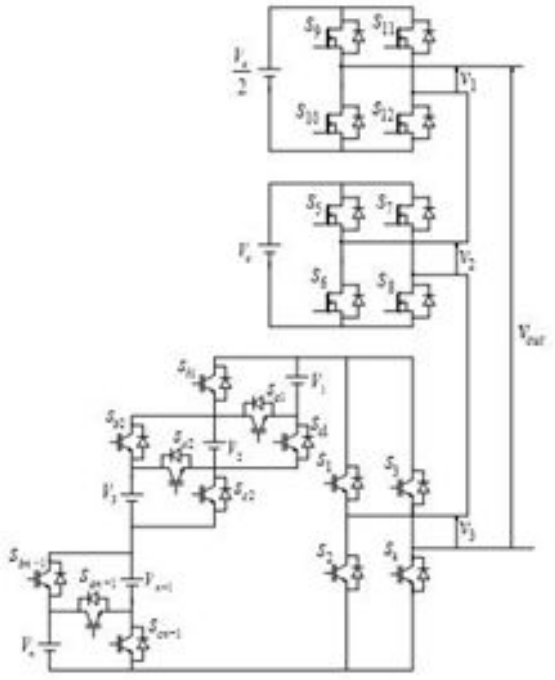


Figure 2. Proposed System for n-level

The proposed system of multilevel inverter for n-level is shown in Figure 2. It consists of three bridges that are two upper H-bridges and the lower H-bridge with series/parallel circuit, which are cascaded. The principle of operation of lower H-bridge with series/parallel circuit is shown in table 2. By using this principle high numbers of steps are obtained at output.

TABLE 2. PRINCIPLE OF OPER. OF SERIES/PARALLEL CIRCUIT

In a conventional cascaded multilevel inverter, the number of output phase voltage levels is defined by, n= 2m+1, where m is the number of dc voltage sources. Each H-bridge requires a dc source and 4 switches. 12 switching devices are needed for 7 levels, 16 switching devices are needed for 9 levels, and 20 switching devices are needed for 31 levels, which make an inverter complicated.

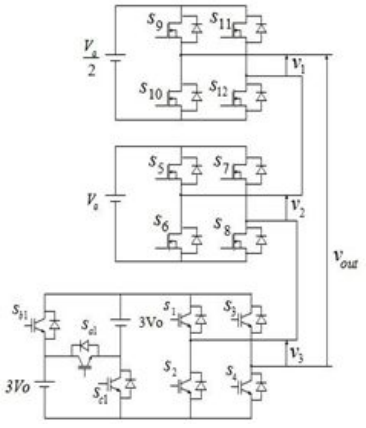


Figure 3. For 31-level output.

But the proposed inverter outputs 12n +7 levels, where n is number of dc voltage sources in series/parallel circuit. Total number of switching devices required is 3n + 9, which makes the output voltage of the inverter almost sinusoidal. Figure 3. shows the proposed topology for 31 level output, it consists of 2 voltage sources in the series/parallel circuit.

Assuming the voltage ratio for 31 level cascaded multilevel inverter voltage sources as 1:2:6, the inverter requires 15 switching devices for 31 levels, which is shown in Figure 3. Two voltage sources are required in series/parallel circuit, levels are obtained by the Eq. (1) and the switching sequence is shown in Table 3.

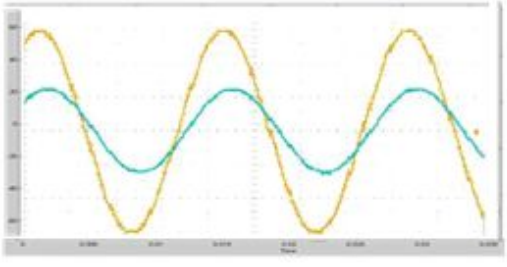
$= 1+2+3$ (1)

TABLE 3. SWITCHING SEQUENCE FOR 31 LEVEL OUTPUT

Switches closed	Vout
S2,S4,S6,S8,S10,S12	0
S9,S12	0.5Vo
S5,S8	Vo
S5,S8,S9,S12	1.5 Vo
Sc1,S1,S4,S6,S7	2 Vo
Sc1,S1,S4,S10,S11	2.5 Vo
Sc1,S1,S4	3 Vo
Sc1,S1,S4,S9,S12	3.5 Vo
Sc1,S1,S4, S5,S8	4 Vo
Sc1,S1,S4,S5,S8,S9,S12	4.5 Vo
Sa1,S1,S4,S6,S7	5 Vo
Sa1,S1,S4,S10,S11	5.5 Vo
Sa1,S1,S4	6 Vo
Sa1,S1,S4,S9,S12	6.5 Vo
Sa1,S1,S4,S5,S8	7 Vo
Sa1,S1,S4,S5,S8,S9,S12	7.5 Vo
S10,S11	-0.5 Vo
S6,S7	- Vo
S6,S7, S10,S11	-1.5 Vo
Sc1, S2,S3,S5,S8	-2Vo
Sc1, S2,S3, S9,S12	-2.5 Vo
Sc1, S2,S3	-3 Vo
Sc1, S2,S3, S10,S11	-3.5 Vo
Sc1, S2,S3, S6,S7	-4 Vo
Sc1,S2,S3,S6,S7,S10,S11	-4.5 Vo
Sa1,S2,S3,S5,S8	-5 Vo
Sa1,S2,S3, S9,S12	-5.5 Vo
Sa1,S2,S3	-6 Vo
Sa1,S2,S3, S10,S11	-6.5 Vo
Sa1,S2,S3, S6,S7	-7 Vo
Sa1,S2,S3, S6,S7,S10,S11	-7.5 Vo

DESIGN AND ANALYSIS

The Matlab/Simulink model of the proposed inverter for 31 level output is shown in Figure 4. It consists of two upper H-bridges are cascaded with lower H-bridge of series/parallel circuit. Simulation is performed for the proposed circuit with MATLAB/SIMULINK.



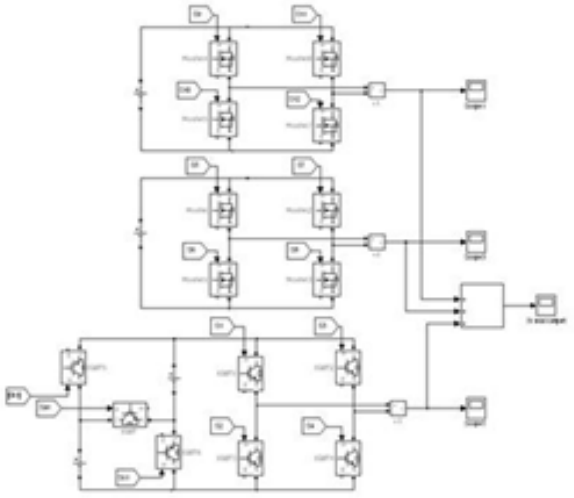


Figure 4. Mat lab/Simulink model for 31 level output.

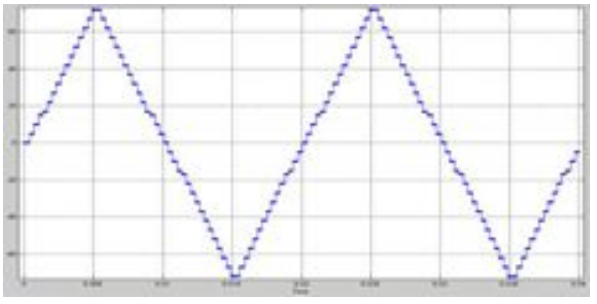


Figure 5. Simulation result for 31 level output.

5V for first upper H-bridge, 10V for second upper H-bridge, and two voltage sources of series/parallel circuit are 30V each maintaining the ratio of 1:2:6, then the amplitude of the inverter's output voltage waveform for 31 levels is 73.3V.

Figure 6. Experimental 31-level output voltage and current.

Figure 5 and Figure 6 shows the 31 level output Voltage and current Waveforms without PWM. It is clear that as the number of level increases, distortion reduces. Switches required in the proposed topology compared to other topologies are shown in figure 7.

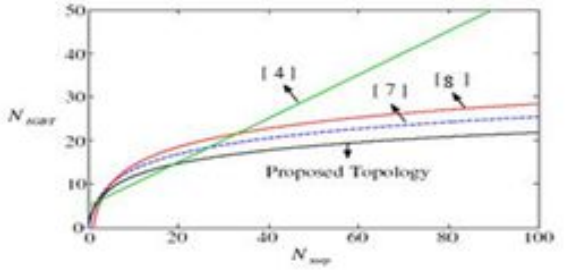


Figure 7. Comparison with other topologies

From the above figure it is shown that less number of switches are required in the proposed topology. Hence complexity is reduced for high number of levels.

VOLTAGE BALANCING

Asymmetric multilevel inverters have the same topology as symmetric multilevel inverters. They differ only in the rating of input dc voltages and control strategies. For many applications it is troublesome to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H-bridge multilevel inverter, Asymmetrical configuration is proposed which uses lesser number of bridges. This scheme therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency. Although the cascaded converter has an inherent self-balancing characteristic, a slight voltage imbalance can occur because of the circuit component losses. Obviously, the primary attraction of the Cascaded Multilevel converter topology is its modularity. However, Cascaded topology requires an excessive amount of DC voltage sources. The most important factors causing the voltage imbalance among these DC capacitors are the difference in the power stage losses and the component tolerances. The internal losses may be differently influenced by the switching and conduction activity and the component tolerances. To achieve steady-state, balanced voltages, these DC capacitors must have the same amount of real power utilization in a given period of time. Due to sharing the same output current, the differences in the capacitor currents are caused by the different duty cycles, because a capacitor current is a product of a duty cycle and an output current. Therefore, the average switching functions or duty cycles in these H-bridge converters must be identical.

VOLTAGE-BALANCING TECHNIQUE

The Cascaded Multilevel Inverter with its use of several voltage sources is suitable in Electric Vehicles (EV) since battery cells is the power source. The battery cells may not always be equal and depending on the output demand the cells may be discharged unequally. The above proposed topology is composed of series basic units which are consisted of series and parallel connections of dc voltage sources. The values of the dc voltage sources differ from one unit to another. Even though the same output voltages are generated, the currents flowing in the circuits have different paths. This means that different DC capacitors see different current waveforms. Consequently, the DC capacitors have different voltage profiles. It is therefore important to investigate the voltage source unbalance problem in the Cascaded Multilevel Inverters. The current direction and if voltage amplitude is negative or positive. If, for example, a capacitor in a full-bridge module for the Cascaded Multilevel Inverter (CMI) has a higher charge (and therefore higher potential) that certain module can be given the heaviest workload during a period where the capacitor is going to be discharged (positive voltage and current owing to the load), lowering the voltage closer to the wanted value. The strategy can also work the other way around, to charge capacitors with lower potential by connecting them to the load, with positive potential forward, when current is owing from the load, or vice versa. However, this strategy is most effective when transferring active power. When transferring only reactive power the sources does not get unbalanced and this balancing strategy is not necessary.

DESIGN EXAMPLE

Voltage balancing technique is well explained with this following example, in which the simulation model shown for 5-level cascaded multilevel inverter.

The Cascaded Multilevel Inverter (CMI) with its use of several voltage sources is suitable in Electric Vehicles (EV) since battery cells is the power source. The battery cells may not always be equal and depending on the output demand the cells may be discharged unequally. It is therefore important to investigate the voltage source unbalance problem in the Cascaded multilevel inverter.

The 5 level CMI shown in above figure 8. is connected to an active/mixed power load and a pure reactive power load can be seen. Each capacitor where charged to 500V during the beginning of the simulation with the charging voltage source. The charging voltage source where disconnected after the circuit reached steady-

state operation. It should be noted that there are battery models connected to each module capacitor, recharging them over time so that they do not run out of stored energy.

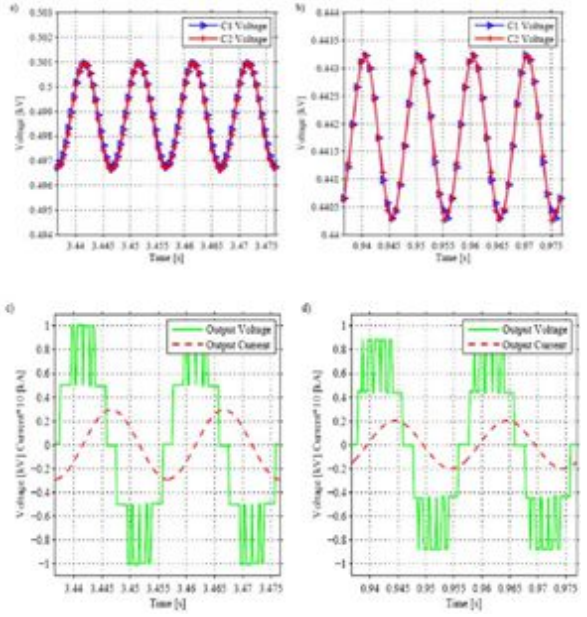


Figure 9. Simulation results of 5level CMI.
a)reactive power transfer capacitor voltages.
b)Active/mixed power transfer capacitor voltages.
c)Reactive power transfer load voltage and current.
d)Active power transfer load voltage and current.

CONCLUSION

Cascaded multilevel inverters in addition to acceptable reliability and simple control, provide a better voltage waveform than the other types of multilevel inverters. In this paper, a new cascaded multilevel inverter topology was proposed which was connected to the dc voltage sources in series and parallel. The suggested topology needs less number of switching devices with minimum standing voltage. THD is also reduced without using modulation techniques. And the proposed topology shows how to operate the Cascaded multilevel inverter without any voltage unbalance problems. The simulation results are shown which are accorded with the theoretical results. The proposed inverter is used in high power applications like EV and HEV drives.

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