

A NOVEL MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

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ABSTRACT

This paper presents the comparison of various Pulse Width Modulation (COPWM) Strategies for the chosen three phase Cascaded Multi Level Inverter (CMLI). Various new schemes adopting the constant switching frequency and also variable switching frequency multicarrier control freedom degree combination concepts are developed and simulated for the chosen three phase CMLI. The three phase CMLI is controlled in this paper with Sinusoidal PWM (SPWM) reference along with Carrier Overlapping (CO) techniques and simulation is performed using MATLAB-SIMULINK. The variation of fundamental RMS output voltage and total harmonic distortion is observed for various carrier overlapping techniques. Among the various equal amplitude carrier overlapping techniques such as COPWMA, COPWMB, COPWMC, and COPWMD, it is observed that COPWMC provides less Total Harmonic Distortion (THD) and COPWMD provides relatively higher RMS voltage. Among the various Variable Amplitude COPWM (VACOPWM) techniques, such as VACOPWMA, VACOPWMB, VACOPWMC, and VACOPWMD, it is inferred that VACOPWMC provides less THD and VACOPWMB provides higher RMS voltage. It is also found that VACOPWM strategies perform better than corresponding COPWM strategies.

KEYWORDS : VACOPWMA, VACOPWMB, VACOPWMC and VACOPWMD.

INTRODUCTION

Multi-Level Inverter (MLI) is a power electronic system that produces a desired sinusoidal output voltage from several levels of DC input voltages. Compared with two level voltage source inverter, multilevel inverter normally provides output voltage with less Total Harmonic Distortion (THD), lower voltage stress of devices, lower electromagnetic interference, low level of high frequency noise, higher RMS voltage and lower common-mode voltage.

The function of the inverter is to change a DC input voltage to a near sinusoidal output voltage of desired magnitude and frequency. So, it is recently used in medium high voltage and high power applications. Multi Level Inverters (MLI) is used for obtaining a near sinusoidal signal (AC) from DC input source. As it is simple to implement and eliminate the number of transformers, minimizes the filter requirements and improves the harmonic quality of the output voltage, MLI is extensively used in compressors, synchronous motors, converters and power generation plants. MLI based DC-AC converter has many advantageous features over the conventional PWM inverter, so it is becoming very attractive in electronic power conversion system.

When used as inverter, MLI offers better output waveform in comparison with two level PWM inverter and if used as active rectifiers, they allow accurate power factor correction and better approximation of sinusoidal currents.

Among many other conventional configurations such as Diode Clamped Multi Level Inverter (DCMLI), Flying Capacitor Multi Level Inverter (FCMLI), it is observed that Cascaded Multi Level Inverter (CMLI) provides high performance with less THD and uses less number of power electronic components. Cascaded Multi Level Inverter is being used popularly, since it can achieve a high range of voltage and power and it has several advantages compared with other conventional inverters such as low THD that eliminate the need of output filters, reduced common-mode and derivative voltages (dv/dt) which can reduce motor insulation, damage and jerks in torque. Three phase CMLI consists of series connection of single-phase H-bridge cells with several separate DC sources. Among the basic MLI topologies, cascaded H-bridge is preferred by its modular structure and linear relationship between the number of inverters elements and levels. But the demand is that large number of DC sources is needed. The fixed DC input voltage which

is not controllable can be modified into variable output voltage by varying the gain of the inverter which can be achieved by Pulse Width Modulation (PWM) strategies.

MULTILEVEL INVERTER

Figure 1 shows a configuration of the three phase five level cascaded multilevel inverter. Cascaded multilevel inverter consists of a series of H bridge inverter units. The general function of this inverter is to produce a desired voltage from Several Separate DC Sources (SDCS). The load voltage is equal to the sum of the output voltage of the respective modules that are connected in series. The number of modules (M) that is equal to the number of DC sources required depends on the total number of positive, negative and zero levels (m) of the CMLI. It is usually assumed that m (number of levels) is odd as this would give an integer valued M (number of modules). In this work, load voltage consists of five levels which include +2Vdc, +Vdc, 0, -Vdc and -2Vdc and the number of modules required is 2. The following equation gives the relation between M and m,

$$M = \frac{m-1}{2}$$

The gate signals for chosen five level cascaded inverter are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index ma and for various PWM strategies. The simulation results presented in this work are compared and evaluated for finding the better technique.

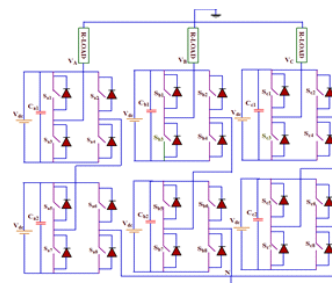


Figure 1 Three phase cascaded multilevel inverter

MODULATION STRATEGIES

In this paper, sinusoidal reference with various overlapping triangular carriers are chosen to produce the desired output. The function of any inverter is to change a DC input voltage to a near AC output voltage of desired magnitude and frequency which can be achieved by various modulation strategies. The number of triangular carriers needed for m level inverter is m-1. Eight different modulation strategies are taken for study to provide increased output voltage and also reduced THD by controlling the on and off time of PWM signal. It is generally recognized that, increasing the switching frequency of the PWM pattern results in reducing lower frequency harmonic waveforms of practical inverters which are non-sinusoidal and contain harmonics, so analysis is performed in order to choose the proper PWM strategy.

This paper focuses on eight different COPWM strategies that utilize the Control Degree Freedom (CFD) combination of vertical offsets among triangular carriers. They are: COPWM-A, VACOPWM-A, COPWM-B, VACOPWM-B, COPWM-C, VACOPWM-C, COPWM-D, and VACOPWM-D. The chosen eight different modulation strategies are simulated in this work and the comparisons are made among them to choose the better technique which will be efficient and provides the output with improved power quality. Carriers are chosen above and below the zero reference line with same amplitude of $A_c = 1.6$ in case of the three basic COPWM techniques and the other four are VACOPWM technique in which the amplitude of first carrier is chosen as 50% of the basic COPWM method and amplitude of the second carrier is 125% of the basic COPWM strategy and the same procedure is repeated below the zero reference line.

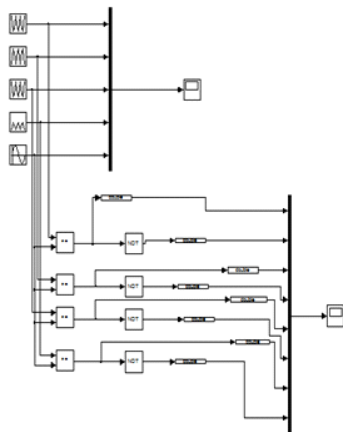


Figure 2 A sample SIMULINK model developed for chosen three phase multilevel inverter for VACOPWM-1 technique

TOPOLOGY AND OPERATION

The five-level hybrid cascaded inverter configuration is shown in Figure 3. By closing the appropriate switches, each H-bridge inverter can produce five different voltages $2V_{dc}$, V_{dc} , 0 , $-V_{dc}$, $-2V_{dc}$, depending on which switches that are switched on. The DC source is connected to all phase legs of the conventional three-phase, two-level inverter and the H bridge cell utilizes a capacitor as a voltage source. Assuming that the DC voltage is equal to $2V_{dc}$, then the voltage of the capacitor of the H-bridge cell has to be maintained to V_{dc} so that a five-level waveform is synthesized in the output. Considering a split DC source, the output of the two-level leg can be equal to either $+V_{dc}$ or $-V_{dc}$.

The voltage of the capacitor is affected during the converter states that the capacitor is connected to the load. These converter states occur during when the output voltage levels are $+2V_{dc}$ and $-2V_{dc}$ and during the zero voltage level. The capacitor is connected in such a way so that its voltage is opposite to the voltage of the lower phase-leg. Selection of the switching state is performed so that, together with the direction of the load current, the voltage of the floating capacitor is regulated within the predetermined limits.

To achieve the different voltage levels in the output a setup of switching state combinations are used. In Table 1 the different states for the five-level CHB inverter are shown. Note that there is the possibility to only turn on and (off) every switch once per cycle, meaning that the inverter can generate a stepped sinusoidal waveform with a fundamental switching frequency.

From Table 1 it can be seen that for the voltage $+2V_{dc}$ switches S_2 , S_3 and S_5 are turned on. When switches S_1 , S_2 and S_5 are closed, the output voltage is $+V_{dc}$. When either the switches S_2 , S_3 and S_6 or the switches S_1 , S_4 , S_5 are closed, the output voltage is 0 . When the switches S_1 , S_2 and S_6 are closed, the corresponding output voltage is $-V_{dc}$. When the switches S_1 , S_4 and S_6 , the output voltage is $-2V_{dc}$.

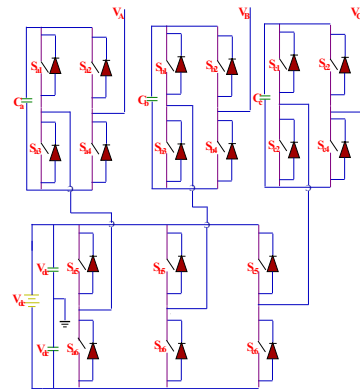


Figure 3. Three-phase, five level hybrid cascaded inverter.

TABLE - 1
Output Voltage and Switching states of five-level hybrid cascaded inverter.

Vphase	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6
$+2V_{dc}$	0	1	1	0	1	0
$+V_{dc}$	1	1	0	0	1	0
0	0	1	1	0	0	1
$-V_{dc}$	1	1	0	0	0	1
$-2V_{dc}$	1	0	0	1	0	1

TABLE - 2
Comparison between conventional CMLI and Cascaded hybrid inverter

Type	Conventional CMLI	Chosen hybrid cascaded inverter
No. of switches	24	18
No. of clamp diodes	24	18
No. of DC sources	6	4

FEATURES OF CHBMLI

For real power conversions from dc to ac and dc to ac, the cascaded inverter need separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell and biomass.

PWM STRATEGIES WITH DIFFERENT PHASE RELATIONSHIPS

We have used the intersection of a sine wave with a triangular wave to generate firing pulses. There are several modulation strategies possible for multilevel inverters. Here multicarrier modulation techniques with sine reference are presented. Number of triangular wave is compared with a controlled sinusoidal modulating signal. The number of carriers required to produce the m level output is m-1. Multiple degrees of freedom are available in carrier based multilevel PWM. Degrees of freedom of exist in frequency, amplitude, phase, DC offset and multiple third harmonic content of carrier and reference signal. This work uses the overlapping vertical

distance between each carrier is $Ac/2$ for eight COPWM techniques and $Ac/4$ for eight VACOPWM. VACOPWM techniques uses the different carrier amplitude which further reduces the THD and increases the RMS fundamental voltage. The reference wave has the amplitude Am and frequency fm . This Am and fm is considered in the middle of the carrier signals. The frequency ratio mf is defined in the carrier overlapping method as follows.

$$m = \frac{fc}{fm}$$

There are sixteen alternative strategies to implement this. They are as given below

CONVENTIONAL CARRIER OVERLAPPING TECHNIQUES

- Carrier Overlapping PWM (COPWMA) strategy.
- Carrier Overlapping PWM (COPWMB) strategy.
- Carrier Overlapping PWM (COPWMC) strategy.
- Carrier Overlapping PWM (COPWMD) strategy.

VARIABLE AMPLITUDE CARRIER OVERLAPPING TECHNIQUES

- Variable Amplitude COPWMA (VACOPWMA) strategy.
- Variable Amplitude COPWMB (VACOPWMB) strategy.
- Variable Amplitude COPWMC (VACOPWMC) strategy.
- Variable Amplitude COPWMD (VACOPWMD) strategy.

Carrier Overlapping PWM-C Strategy

In COPWM-C technique, the positive group carrier are arranged such that the alternate carriers are displaced from the adjacent by 180 degree i.e. the alternate carriers are phase opposing. Similarly carrier group are displaced 180 degree from its adjacent one as shown in Figure 4

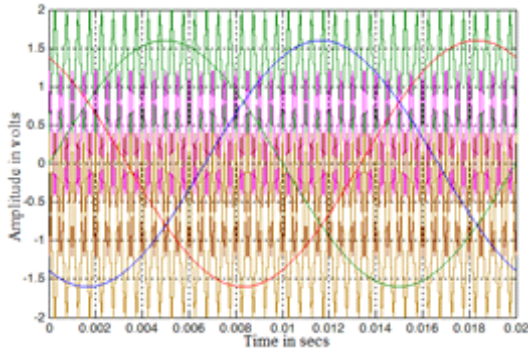


Figure 4 Modulating and carrier waveforms for COPWM-C strategy ($ma=0.8$ and $mf=40$)

Carrier Overlapping VAPWM-C Strategy

In this method all the carriers have the same frequency and the different amplitude of carrier overlapping with each other. All the carriers are alternatively in position which is shown in Figure 5 There is phase shift of 180 degree between adjacent carriers.

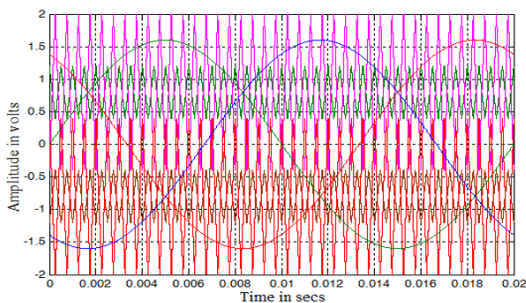


Figure 5 Carrier arrangement for COPWMC strategy ($ma = 0.8$)

and $mf=40$).

SIMULATION RESULTS

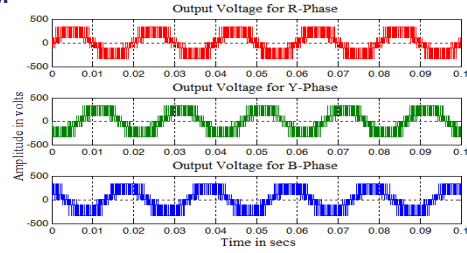


Figure 6 Output voltage generated by COPWMA technique for R-load ($ma=0.8$).

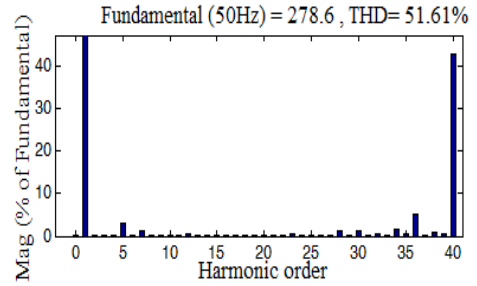


Figure 7 FFT plot for output voltage of COPWMA technique.

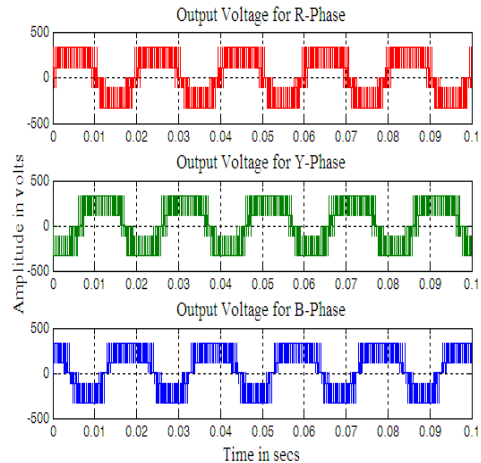


Figure 8 Output voltage generated by VACOPWMA technique for R-load ($ma=0.8$).

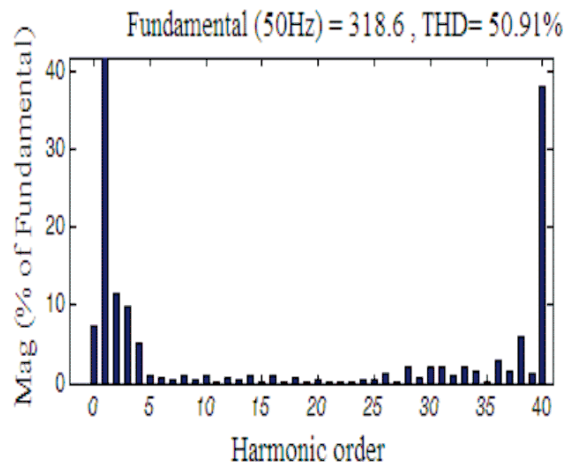


Figure 9 FFT plot for output voltage of VACOPWMA technique.

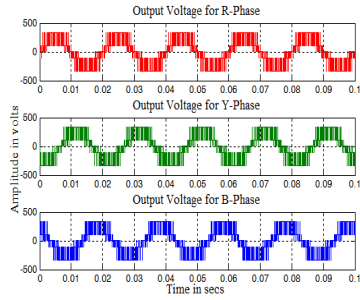


Figure 10 Output voltage generated by COPWMB technique for R-load (ma=0.8).

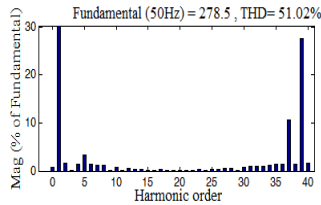


Figure 11 FFT plot for output voltage of COPWMB technique.

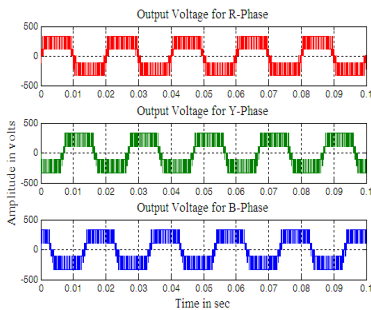


Figure 12 Output voltage generated by VACOPWMB technique for R-load (ma=0.8).

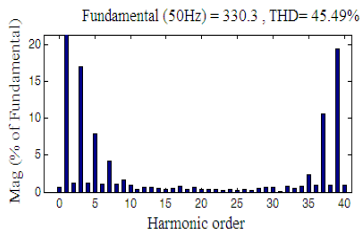


Figure 13 FFT plot for output voltage of VACOPWMB technique.

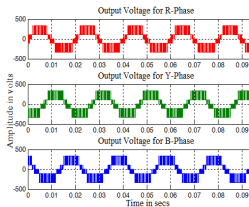


Figure 14 Output voltage generated by COPWMC technique for R-load (ma=0.8).

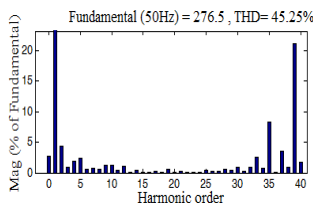


Figure 15 FFT plot for output voltage of COPWMC technique.

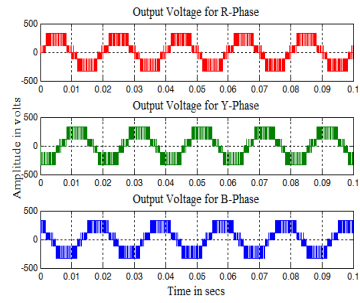


Figure 16 Output voltage generated by VACOPWMC technique for R-load (ma=0.8).

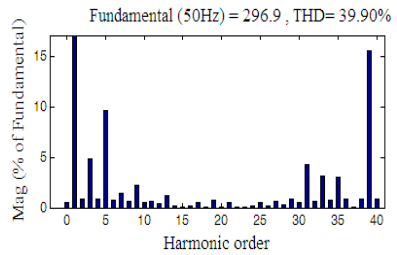


Figure 17 FFT plot for output voltage of VACOPWMC technique.

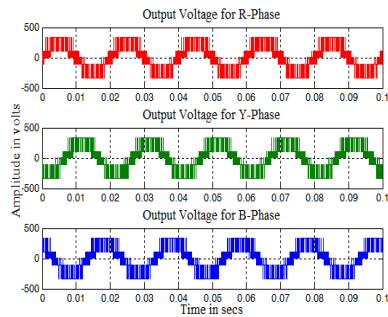


Figure 18 Output voltage generated by COPWMD technique for R-load (ma=0.8).

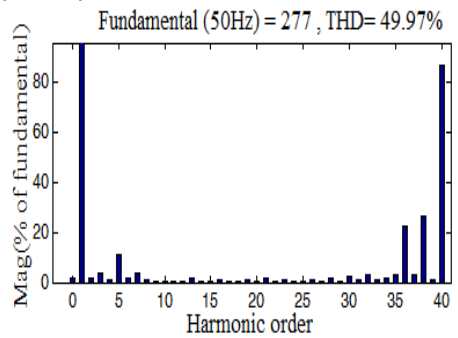


Figure 19 FFT plot for output voltage of COPWMD technique.

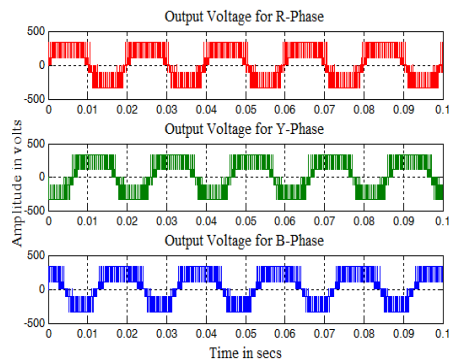


Figure 20 Output voltage generated by VACOPWMD technique for R-load (ma=0.8).

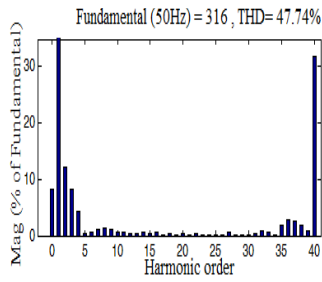


Figure 21 FFT plot for output voltage of VACOPWMD technique.

TABLE – 3
%THD comparison for different modulation indices for R-load.

%THD	ma				
	1	0.9	0.8	0.7	0.6
COPWMA	36.68	44.20	51.61	59.95	69.54
VACOPWMA	39.63	45.14	50.91	56.95	65.71
COPWMB	36.26	43.73	51.02	58.97	68.80
VACOPWMB	36.71	41.57	45.49	49.95	53.33
COPWMC	31.57	38.53	45.25	51.01	56.14
VACOPWMC	29.00	34.75	39.90	45.67	54.02
COPWMD	35.18	42.59	49.97	57.37	66.72
VACOPWMD	36.87	42.79	47.74	53.4	60.83

TABLE – 4
VRMS comparison for different modulation indices for R-load.

VRMS	ma				
	1	0.9	0.8	0.7	0.6
COPWMA	238.4	218.2	197.0	173.4	150.5
VACOPWMA	254.7	239.8	225.3	209.4	190.1
COPWMB	238.1	218.4	196.9	173.5	150.6
VACOPWMB	259.6	246.1	233.6	220.2	206.1
COPWMC	237.1	216.9	195.5	171.5	147.3
VACOPWMC	246.0	228	210	188.1	156.6
COPWMD	237.5	217.2	195.9	171.8	147.4
VACOPWMD	253.2	238.4	223.4	206.1	185.4

CONCLUSION

A hybrid cascaded symmetrical inverter has been proposed in this paper. The most important feature of the system is being convenient for expanding and increasing the number of output levels simply with less number of switches. This method results in the reduction of the number of switches, losses and cost of the converter. Performance indices like %THD, VRMS (indicating the amount of DC bus utilization), CF and FF related to power quality issues have been evaluated, presented and analyzed. Based on presented switching algorithm, the chosen multilevel inverter generates near sinusoidal output voltage and as a result, has relatively low harmonic content for the VACOPWMC strategy but provides higher DC bus utilization with VACOPWMB technique. Table III and IV shows the total harmonic distortion and RMS for all chosen modulating indices. Table V displays form factor for all modulating indices. Table VI shows crest factor for all chosen modulating indices.

REFERENCES

1. K.A. Corzine, M.W. Wielebski, F.Z. Peng and J. Wang, "Control of Cascaded Multi-Level Inverters", Process. IEEE conf Rec. 0-7803-7817-2/03, pp.1549-1555.
2. A. Radan, A. H. Shahirinia and M. Falahi, "Evaluation of Carrier-Based PWM Methods for Multi-level Inverters", Process. IEEE conf Rec. 1-4244-0755-9/07, pp. 389-394.
3. K.Arab Tehrani, H.Andriatsioharana, I.Rasoanarivo and F.M.Sargos, "A Novel Multilevel Inverter Model", Process. IEEE conf Rec. 978-1-4244-1668-4/08, pp.1688-1693.
4. Pablo Lezana, José Rodríguez and Diego A. Oyarzún, "Cascaded Multilevel Inverter With Regeneration Capability and Reduced Number of Switches", IEEE Transactions on Industrial Electronics, vol. 55, no. 3, March 2008, pp.1059-1066.
5. [5] Manyuan Ye , Pinggang Song , and Chaowei Zhang, "Study of Harmonic Elimination Technology for Multi-level Inverters", Process. IEEE conf Rec. 978-1-4244-1718-6/08, pp.242-245.

6. Domingo Ruiz-Caballero, Luis Martinez, Reynaldo Ramos and Samir A. Mussa, "New Asymmetrical Hybrid Multilevel Voltage Inverter", Process. IEEE conf Rec. 978-1-4244-3370-4/09, pp. 354-361.
7. Georgios S. Konstantinou and Vassilios G. Agelidis, "Performance Evaluation of Half-Bridge Cascaded Multilevel Converters Operated with Multicarrier Sinusoidal PWM Techniques", Process. IEEE conf Rec. 978-1-4244-2800-7/09, pp.3399-3404.
8. Arif Al-Judi, Hussain Bierk and Ed Nowicki, "A Modified Cascaded Multilevel Inverter With Reduced Switch Count Employing Bypass Diodes", Process. IEEE conf Rec. 978-1-4244-2601-0/09, pp. 742-747.
9. Georgios S. Konstantinou, Sridhar R. Pulikanti and Vassilios G. Agelidis, "Harmonic Elimination Control of a Five-Level DC-AC Cascaded H-bridge Hybrid Inverter" Process. IEEE conf Rec. 978-1-4244-5670-3/10, pp. 352-357.
10. Mariusz Malinowski, K. Gopakumar, Jose Rodriguez, and Marcelo A. Pérez, "A Survey on Cascaded Multilevel Inverters", IEEE Transactions on Industrial Electronics, vol. 57, no. 7, July 2010, pp.2197-2206.
11. Rokan Ali Ahmed, S. Mekhilef and Hew Wooi Ping, "New multilevel inverter topology with reduced number of switches", International Middle East Power Systems Conference (MEPCON'10) December 19-21, 2010, pp.565-570.
12. Domingo Ruiz-Caballero, Rene Sanhueza, and Marcelo Lobo Heldwein, "Symmetrical hybrid multilevel inverter concept based on multi-stage switching cells", Process. IEEE conf Rec. 978-4577-1646-1/11 pp.746-781.
13. Suroso and Toshihiko Noguchi, "A Multilevel Voltage-source Inverter Using H-Bridge and Two-Level Power Modules with a Single Power source", Process. IEEE conf Rec. 978-1-4577-0001-9/11, pp. 262-266.
14. Alessandro Luiz Batschauer, Samir Ahmad Mussa and Marcelo Lobo Heldwein, "Three Phase Hybrid Multilevel Inverter Based on Half-Bridge Modules", IEEE Transactions on Industrial Electronics, vol. 59, no. 2, February 2012, pp. 668-678.
15. C. R. Balamurugan, S. P. Natarajan and V. Padmathilagam, "Comparative Study on Unipolar PWM Strategies for Three Phase Five Level Cascaded Inverter", ISSN 1450-216X Vol. 80 No. 4 (2012), pp.517-539.
16. Ehsan Najafi and Abodul Halim Mohamed Yatim, "Design and Implementation of a New Multilevel Inverter Topology", IEEE Transactions on Industrial Electronics, vol. 59, no. 1, 2012, pp.4148-4154.