VOLUME-7, ISSUE-1, JANUARY-2018 • PRINT ISSN No 2277 - 8160

Original Research Paper

Engineering

A BUS ENCODING TECHNIQUE FOR MINIMIZING DELAY IN VLSI INTERCONNECTS

Tanu Verma

Electronics and Communication Department Techno India NJR Institute of Technology Udaipur, Rajasthan (India)

ABSTRACT

In a typical bus system of NOC, crosstalk can affect signal delays by changing the times at which signal transitions occur. Hence, Delay reduction is main objective of our current research work. This paper develops a novel technique, in which inter-wire crosstalk considers sufficiently and reduces the delay due to coupling transition approximately up to 13% - 13.63% for 8 bit, 16 bit, 32 bit and 64 bit wide data bus with an additional area penalty. The effectiveness of coding method has been tested using MATLAB. Transmission results are tested on bus of network on chip which is simulated on Xilinx and implemented on FPGA.

KEYWORDS : Crosstalk, Self transition, Coupling Transition, low power switching.

I. INTRODUCTION

Crosstalk can affect signal delays by changing the times at which signal transitions occur. For example, consider the signal waveforms on the cross-coupled nets A, B, and C in figure 1. The transitions on net A and net C can affect the time at which the transition occurs on net B because of capacitive cross-coupling. Contributing to a setup violation for a path containing B, a rising-edge transition on net A at the time shown in figure 1 [15] can cause the transition to occur later on net B. Similarly, the transition can occur earlier on net B, possibly contributing to a hold violation for a path containing B due to the falling-edge transition on net C.

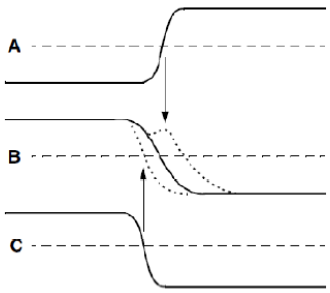

Fig. 1 – Transition slowdown or speedup caused by crosstalk

A victim net is a net that receives undesirable cross-coupling effects from a nearby net. An aggressor net is a net that causes these effects in a victim net. Note that a victim net can also be an aggressor net; and an aggressor net can itself be a victim net. The relationship between two nets being analyzed is referred by the terms aggressor and victim. The timing impact of an aggressor net on a victim net depends on several factors:

- The amount of cross-coupled capacitance.
- The relative times and slew rates of the signal transitions.
- The switching directions (rising, falling).
- The combination of effects from multiple aggressor nets on a single victim net.

Bus encoding technique is introduced to reduce delay by reducing Coupling Transition activity αC.

Techniques to reduce power dissipation and delay were well explored in the literatures like [7] offers a TSC (Two Stage Coding) technique. Literature [8] introduced a technique in which data bus is first divided into two group as odd group and even group and then invert the data or send it as it is according to cases. Paper [9] developed a mathematical model for a memoryless encoding scheme and proposed a novel partitioning method for reducing the transition energy. Literature [10] explored a technique in which input data bits coded in four different ways such as Original Data, Invert Data, Ex-Oring with some code words and Ex-Oring with another code words and then send all the four results in comparator mode, which compares reduction in transition. The lowest of the four results decides the value of encoded data. Literature [11] proposed an octo coding technique to reduce the hamming distance, in which input data bits coded in eight different ways such as Invert, Swap, Invert even position, Invert odd position, Rotate left with invert, Rotate Right with invert, Circular Left Shift and Circular Right Shift based. Technique resulting in maximum reduction in power dissipation and delay, is selected. Technique introduced in paper [6] is Quadro Coding, in this method, the applied input data is coded in four different ways and the coding resulting in maximum reduction in transition activity is selected.

The purpose of present paper is to propose a novel technique, which attempts to reduce the number of effective coupling transitions (1 0 or 0 1) between adjacent bus because in CMOS VLSI circuits, the coupling transitions are responsible for delay.

The rest of the paper is organized as follows: The bus model is explained in section II. The proposed model is well explored in section III. Methodology is explained in section IV. The results and discussions are provided in section V and conclusions are made in section VI.

II. BUS MODEL

The distributed model of DSM bus line, in terms of RLC, is shown in fig.5. The bus lines can be assumed to be lossy, distributed, capacitively and inductively coupled which interact strongly with each other through parasitic capacitances and inductances. In the well-known model of DSM bus lines [12][13] the interconnect coupling capacitance CC is strongly dependent on the inter–wire separation, whereas the lumped grounding capacitance CS is a weak function of inter-wire separation.

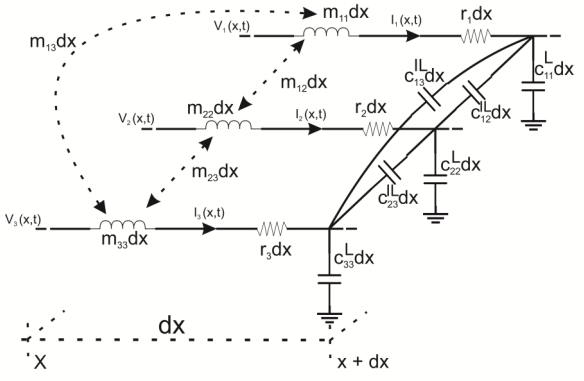

Fig. 5 - RLC Model for DSM Bus

There are some limitations in previous method as no. of transitions was more so as delay was very high.

III. PROPOSED MODEL

The main goal of the proposed scheme is to make data less correlated i.e. to make transitioning of data smoother. The proposed encoding scheme is as follows:

A. Encoder-

Let D be the n bit data on the bus to be transmitted at time t and X be the encoded data. The n bit data on the bus is divided into a subset of four bits from right to left and for each subset count the number of zeroes and ones. Now for encoding purpose nth (right most) bit is encoded as it is i.e. X(n)=D(n), and the following operations are performed to encode rest of data bits from right to left according to different conditions:

X (P) = D (P) XOR X (P+1) (1)
X (P) =D (P) XNOR X (P+1) (2)

Where P gives the position of the data bit varies from n-1 to 1.

1. Start
2. Set Count ones=0, count zeroes =0, count=0.
3. Divide I/P data into subsets of 4 bits each.
4. Count count zeroes AND count count ones.
5. If (Count zeroes > count ones)

Then Encode Rightmost bit as it is.

Set control bit =1
And set X (P) = D (P) XOR X (P+1)
return

6. Else if (Count zeroes < count ones)

Then Encode Rightmost bit as it is.
Set control bit =0
And set X (P) =D (P) XNOR X (P+1)
return

7. Else (count ones= count zeroes)

Then count the number of transition in the subset

8. If (Count transition > 1)

Then Encode Rightmost bit as it is.
Set control bit =1
And set X (P) = D (P) XOR X (P+1)
return

9. E lse

Encode Rightmost bit as it is.
Set control bit =0
And set X (P) =D (P) XNOR X (P+1)
Return

10. End

The control bit of each subset gives information about the operation performed on the corresponding subset. So due to control bit, length of encoded data X would be n+n/4.

B. Decoder-

For the decoding purpose encoded data is again divided into subsets from right to left. Then, nth bit is decoded as it is i.e.

D (n) =X (n) and according to the control bit of each subset, original data is recovered by using anyone of the operation:

D (P) = X (P) XOR X (P+1) (3)
D (P) = X (P) XNOR X (P+1) (4)

Where P gives the position of data bit varies from n-1 to 1.

1. Start
2. Divide encoded seq. into subsets of 4 bits each.
3. Note the control bit for each block.
4. If (control bit =0)

Then decode rightmost bit as it is.
Apply D (P) = X (P) XNOR X (P+1)
Return

5. Else decode rightmost bit as it is.

Apply D (P) = X (P) XOR X (P+1)
Return

6. End

IV. METHODOLOGY

In order to carry out the experiment and the target, following steps were involved.

1. Developed the MATLAB script for the encoder.
2. Developed the MATLAB script for the decoder.
3. For delay analysis, transmission results are tested on bus of network on chip which is simulated on Xilinx and implemented on FPGA.

V. SIMULATION RESULT AND DISCUSSION

Result Analysis for Delay

For delay analysis, transmission results are tested on bus of network on chip which is simulated on Xilinx and implemented on FPGA. The simulation has been tested against approximately 10,000 different input vectors and it was observed delay reduction is guaranteed in all the cases. Table 1 shows the simulation results of 8 bits, 16 bits, 32 bits and 64 bits data and percentage reduction in delay:

TABLE I RESULTS OF % REDUCTION IN DELAY FOR DIFFERENT BUS WIDTH USING DUAL CODING TECHNIQUE

Number of Bits in Data	Original Data	Delay (ns)	Encoded Data	Delay (ns)	% Reduction in Delay
8	00001101	2.853	00000001	2.464	13.63
16	10110100 00101110	4.968	11000011 11100000	4.322	13.00
32	10111000 11010000 11111000 11110000	6.247	00111000 00011111 11111000 00000000	5.396	13.62
64	11110100 10010000 01000010 11110010 11101000 11110101 11110010 00011101	9.758	00000011 10001111 11000001 11111110 00001000 00000011 00000001 11110001	8.435	13.55

VI. CONCLUSION

This paper presents a Novel Technique which makes efforts to reduce delay due to coupling transitions in CMOS VLSI circuits. The proposed technique simply uses XOR and XNOR operations according to conditions to achieve the objective. Results of this novel technique are very efficient and useful to reduce delay by 13% - 13.63% for 8 bit, 16 bit, 32 bit and 64 bit wide data bus with an additional area penalty.

REFERENCES

[1] Paul P. Sotiriadis and Anantha P. Chandrakasan, "A Bus Energy Model for Deep Submicron Technology," IEEE transactions on VLSI systems, vol. 10, no. 3, June 2002.
[2] J.V.R.Ravindra, Navya Chittarvu & M.B.Srinivas, "Energy Efficient Spatial Coding Technique for Low Power VLSI Applications," IEEE, 27-29 Dec. 2006.
[3] Mircea R. Stan and Wayne P. Burleson, "Bus Invert Coding for Low Power I/O," IEEE Transactions on Very Large Scale Integration System, Vol. 3, No.1, March 1995.
[4] Paul P. Sotiriadis and Anantha P. Chandrakasan, "Bus Energy Reduction by Transition

Pattern Coding Using a Detailed Deep Submicrometer Bus Model," IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications, VOL. 50, NO. 10, October 2003.
[5] Deepika Agarwal, G. Nagendra Babu, B. K. Kaushik & S. K. Manhas, "Reduction of Crosstalk in RC Modeled Interconnects with Low Power Encoder," Indian Institute of Technology, Roorkee, 2011 IEEE.
[6] Ojashri Sharma, Aakash Saini , Sandeep Saini & Abhishek Sharma, "A Quadro Coding Technique to Reduce Self Transitions in VLSI Interconnects," IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)2016.
[7] Deepa N.Sarma, G.Lakshminarayanan & K.V.R.Suryakiran Chavali, "A Novel Encoding Scheme for Low Power in Network on Chip links," 25th International Conference on VLSI Design, IEEE, 2012.
[8] J.V.R. Ravindra, K.S. Sainarayanan and M.B. Srinivas, "A Novel Bus Coding Technique for Low Power Data Transmission," 2007.
[9] Ge Chen, Steven Duvall & Saeid Nooshabadi, "Analysis and Design of Memoryless Interconnect Encoding Scheme," IEEE 2009.
[10] Xin Zhao, Xi Tian, ShaoShi Yan & Yongfeng Guan, "A novel low power bus coding technique for nanometer technology," IEEE, 2007.
[11] N. Vithya Lakshmi & M. Rajaram, "An Octo Coding Technique to Reduce Energy Transition in Low Power VLSI Circuits," IJRET: International Journal of Research in Engineering and Technology, Volume: 02, Issue: 11, Nov 2013.
[12] A.Sathish, Dr. M.Madhavi Latha & Dr. K.Lal Kishore, "Efficient Crosstalk Reduction Technique for Data Bus," International Journal of Computer Applications, Volume 28, No.11, August 2011.
[13] C.Raghunandan, K.S.Sainarayanan & M.B.Srinivas, "Area Efficient Bus Encoding Technique for Minimizing Simultaneous Switching Noise (SSN)," International Institute of Information Technology (IIIT), Hyderabad, India 2007 IEEE.
[14] K.S.Sainarayanan, J.V.R.Ravindra, C.Raghunandan and M.B.Srinivas, "Coupling Aware Energy-Efficient Data Scrambling on Memory-Processor Interfaces," Second International Conference on Industrial and Information Systems, ICIIS 2007, 8 – 11 August 2007, Sri Lanka.
[15] J.Venkateswara Rao and A.V.N.Tilak, "A Bus Encoding to Reduce Crosstalk Noise Effect in System on Chip," International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.2, June 2011.