Volume-4, Issue-5, May Special Issue-2015 • ISSN No 2277 - 8160

Research Paper Engineering

A Reliable ALU Based Test Pattern Generation for VLSI chips

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ABSTRACT

ABIST is used to test the fundamental inherent blocks of all digital and logic circuits.In ABIST mechanisms, ALU's mim ics the generation of test patterns.

In contrast to the extisting schemes,areliable ALU-basedtest pattern generation methodology is presented; The proposed method achieves test pattern generation and test response compaction with the help of basic arithemetic blocks like adders and substractors by modifying them. The proposed method generates combination of patterns with weights 0, 0.5, and 1. At-speed testing without degradation in the performance and no space aloft is attained by ALU-based test pattern generation.The hardware overhead of the presented method is less(≈ 75%)when compared to previous ,whilist ALU redesign is not imposed ,that results in test application time reduction of 20%-95%.

KEYWORDS : BIST, Three weights 0-0.5-1, ALU

I. INTRODUCTION

BIST is referred as a design-for-testability method, i.e., capability of a circuit to test it-self . Circuit under test(CUT) can be the whole chip or just a portion of it (e.g The fundamental BIST architecture needs the inclusion of three blocks .: a TPG(test pattern generator), a RA (response analyzer), and a TC(test controller)a memory core or a logic block. BIST can be used for divergent, networked testing of the logic and memory elements of the system.

A necessary component in order to implement self-test is a stimuli generator. There are various test pattern generators(TPG), that the unit being tested is an p-input,q-outputcombinationalcircuit. Very High fault coverage is achieved through Exhaustive pattern BIST which excludes the test generation process.Exhaustive pattern BIST applies all possible 2p-input patterns to the block to test anp-input block of combinational logic. Depending upon the clock rate, exhaustive pattern is usually not feasible if n is larger than about 22.Pseudo-exhaustive testing depends on various forms of circuit sections and attempts to test each sectionthoroughly. Pseudo-random binary order is the representation ofsequence of 0's and 1's .The bits appear to be random , but they are in some way repeatable in this order. The autonomous LFSR(linear feedback shift register)pattern generator is generally used for PRPG(pseudo-random pattern generation). PRPG requires less patterns than exhaustive test, but more patterns than the deterministic ATPG. In PRPG, each bit has equal probability of being a 0 or a 1. The number of patterns applied is typically of the order of 103 to 107 and is related to the circuit's fault coverage and the testability needed.

Hard-to-detect faults are best dealt by Weighted pseudorandom pattern BIST. In a pseudorandom test, each input bit has a probability of 1/2 of being either a 1 or a 0. In this test, the probabilities, or input weights, may vary.Multiple weight value allocations have been recommended because various faults require various biases to be applied to the circuitin the form of the input combinations, to make sure that a relatively lessnumber of patterns can detect all faults.

To reduce the hardware realization cost, othermethods based on a values of 0, 1, or μ (unbiased) is allocated to each scan chain in CUT. The value sets are squeezed and stored on the tester.This approach, has beneficial effect on theutilized power, apart from minimizing the hardware overhead.The inputs for circuit being tested(those having value 0 or 1) remain constant during the specific testof evaluation.From the above it can be concluded that a reliable ALU based test pattern generation make use of weight values 0, 1, and 0.5 that has practical interest since it combines low realization cost with low test time.

The proposed ABIST methodallows at-speed testing while introducing virtually no area aloft and no performance degradation. These characteristics make ABIST applicable for consumer applications where the primary objective is to reduce the form-factor of the products without waiving the performance. The ABIST methodology is also suitable to embedded DSP cores,where it is highlytedious to access consecutive blocks externally.

The proposed methodologyovercomes the problem of area overhead that arises in LFSR based BIST mechanisms. However, the methodology proposed in [4] have three major drawbacks: 1) it works only if the adder is a ripple carry adder of the ALU ; 2) it requires redesigning the ALU; this modification, asideof being costly, requires reconstruct of the data path of core, a method that is generally not encouraged in current BIST methods; and 3) The operating speed of the adder is affected with increased delay. In this paper, a method for ALU based test pattern generation is presented. The proposed methodmeets with the extisting disadvantages of the method proposed in [4]. More exactly:

1) it does not inflict any requirements about the adder design2) it does not need any alteration of the adder; and hence, 3) does not influence or vary the operating speed of the adder. The proposed method compares favourably to the method suggested in [4] and [5] in terms of the required physical componentsaloft.

This paper is arranged in a systematic way as shown. Moving towards Section II, the underlying idea of the ALU based weightedtest pattern generation is shown. Moving towards Section III,generation ofweighted patterns utilizing an ALU design methodology is shown.In section IV,the simula-

tion results were presented. Finally, Section V, concludes this paper.

Table
TEST SET FOR THE C17 BENCHMARK

Test Vector	Inputs A[4:0]
T1	101
T2	1010
T3	10010
T4	11111

Table
TRUTH TABLE OF THE FULL ADDER

@	C_{in}	A[i]	B[i]	S[i]	C_{out}	Comment
1	0	0	0	0	0	
2	**0**	**0**	**1**	**1**	**0**	$C_{out=}$ C_{in}
3	**0**	**1**	**0**	**1**	**0**	$C_{out=}$ C_{in}
4	0	1	1	0	1	
5	1	0	0	1	0	
6	**1**	**0**	**1**	**0**	**1**	$C_{out=}$ C_{in}
7	**1**	**1**	**0**	**0**	**1**	$C_{out=}$ C_{in}
8	1	1	1	1	1	

II.ALU-BASED TEST PATTERN GENERATION

The idea of an ALU-based test pattern generationis illustrated by means of an example. Herethe c17 ISCAS benchmark [6],[7] is considered and the test sets for it is as shown in Table 1.

From this deterministic test set, in accordance to apply the test pattern generation method, one of the methods proposed in [1], [2], and [3] can be used. As stated in these methods, a typical weight value assignment procedure would involve separating the test patternsinto two subgroups, S1 and S2 as follows:

The weight value allocations for these subgroups is000 and 00 , where a "0"denotes a weight value allocationof 0.5, a "1" indicates that the input is constantly operated by the logic "1"value, and "0" value indicates that the input is operated by the logic"0"value. In the first allocation, inputs A[2] and A[0] are constantly operated by "1",while inputs A[4], A[3], A[1] are randomly generated (i.e., have values 0.5). Similarly, in the second weight allocation (subgroups S2),inputs A[0] and A[2] are steadily operated by value "0", the input A[1] is controlled by logic value "1" where as the inputs A[3] , A[4] are produced non-specifically.

The above persuades for a configuration of the ALU, where the following constraints are met: 1) an ALU output can be constantly operated by "1" or "0" and 2) an ALU cell with its output constantly operated to logic value "0" or logic value "1" permits the Cin (carry input) of the stage to shift to its Cout (carry output) unchanged. This hindmost condition is needed to effectively producedeterministic patterns in the ALU outputs whose weight value allocation is "0".

III. DESIGN APPROACH

The implementation of this method depends on truth table of the full adder, as shown in Table 2.Therefore it is sufficient to setthe in lines in table 2 i.e.,2,3,6,7 for shifting the values from Cin(Carry input) to Cout (carry output). The design approach is based on this observation.

The proposed design approach is implemented based on the ALU cell shown in Fig. 1.The ALU unit comprisesof a Full Adder (FA) block and a D-type flip-flop block.The output is given to one of the full adder block inputswith set and reset asynchronous inputs of D flip -flop. In ALU unit,WOLOG,the set and reset are active high values (assumption). In the same figure the respective unit of thedriving ALU,B[i] register is also presented. For this ALUunit, one out ofthree possibilities can be used, as shown in Fig. 2.

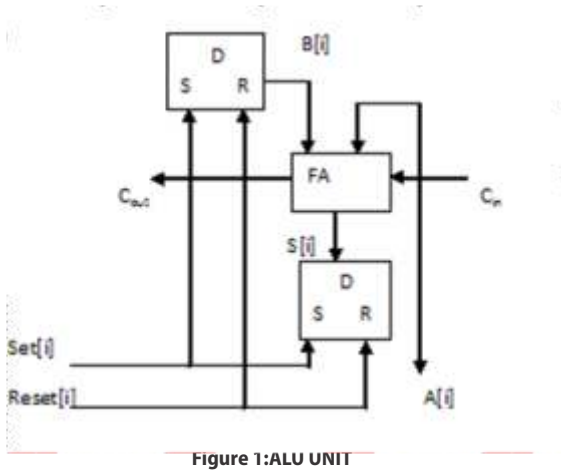


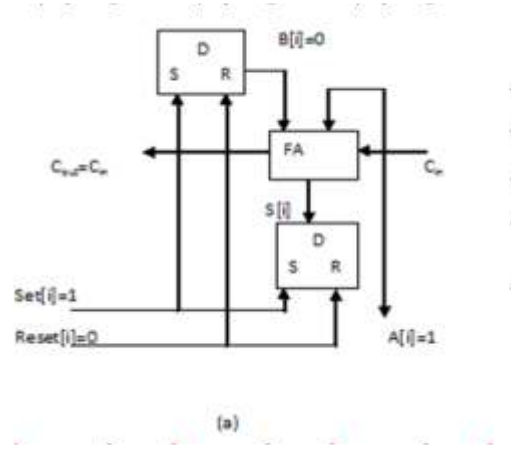
Figure 1:ALU UNIT

OPERATION OF THE ALU UNIT:

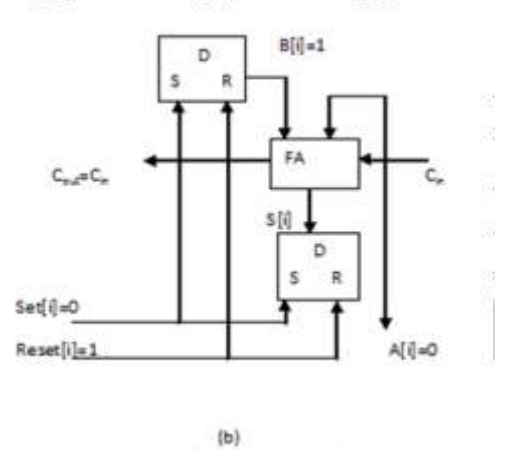
1. For possibility presented in Fig.2 (a) Considering A[i] =1 , The output equals to 1for reset[i]=0 and set[i]=1 ,hence B[i]=0 and A[i]=1. Cin will be equal to Cout and Cin is transferred to the Cout.

2. For possibility presented in Fig.2(b) Considering A[i] =0 , The output equals to 0 forreset[i]=1 and set[i]=0 . Hence B[i]=1 and A[i]=0 . In this case Cinequal to Cout. The value of Cin is shifted to the Cout.

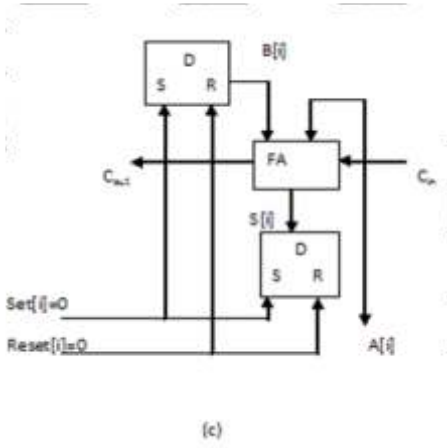
3.For possibility presented in Fig.2(c) Considering A[i] = "-" , set[i] =0 and reset[i] =0.To producedesired random patterns to the inputs of the Circuit to be tested,the D flip-flop input of register B is operated by either 1 or 0.Depending on that value,will get added up to the inputs of ALU.



(a)



(b)



(c)

Figure2:Possibilities of the ALU unit of Fig. 1.

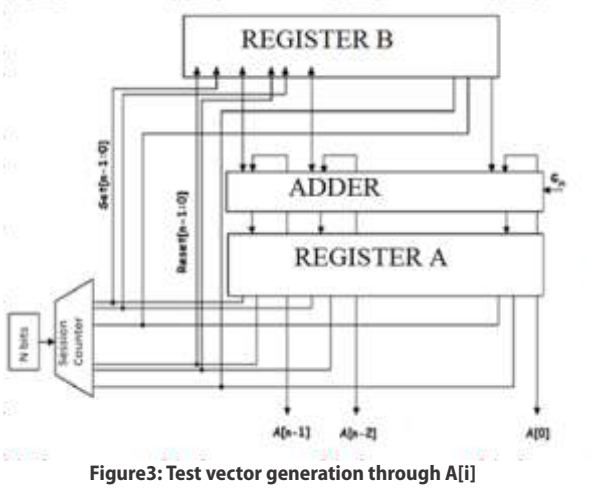


Figure3: Test vector generation through A[i]

In Fig. 3, the general arrangement of elements of the proposed methodology is presented. The Reset[n-1:0] and Set[n-1:0] signals drives the R and S inputs of the Register A & B provided by the Logic module. The signals that operate the R inputs of the flip-flopsof Register B, also operate the S inputs of the flip-flops ofRegister A and vice versa.

IV.RESULTS

Verilog code is generated for this ALU circuit using SPARTAN 3E.Then RTL schematic is produced using XILINX 14.2.These are executed and implementedon FPGA SPARTAN 3.

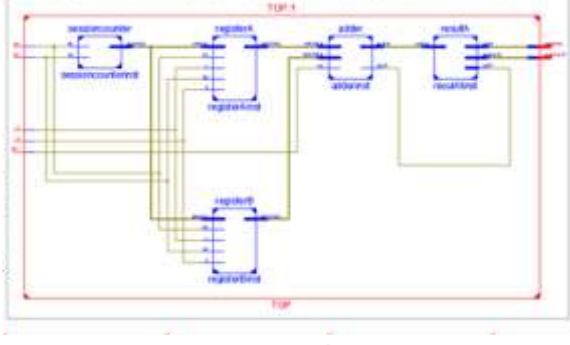


Figure3.1:Existing schematic RTL

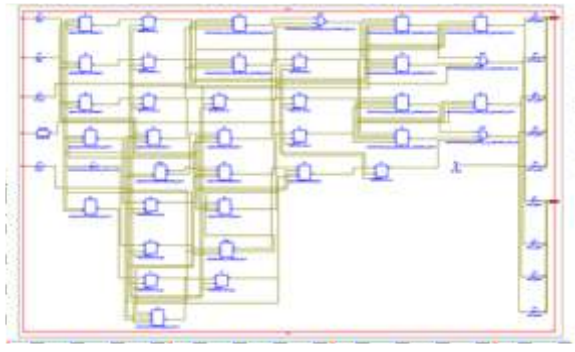


Figure3.2: Existing tech.schematic

Figure3.3: Existing output wave

In this method clk, rst are used to set the register contents. given S=1,R=0 are used to set the D-flip flop.

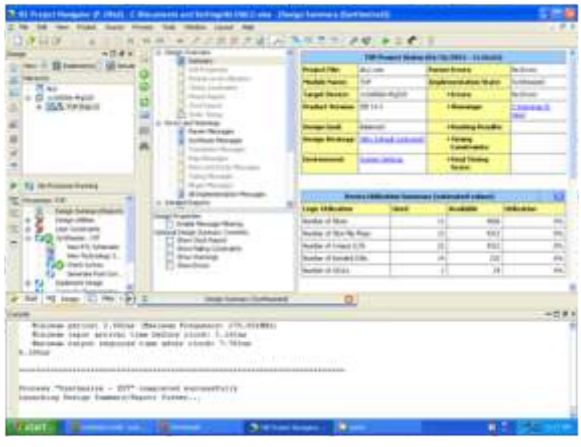


Figure3.4: Existing device summary

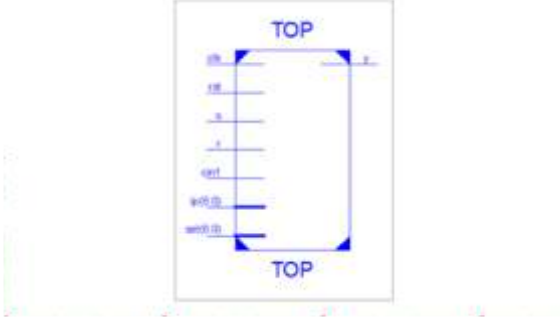


Figure3.5: Proposed top module

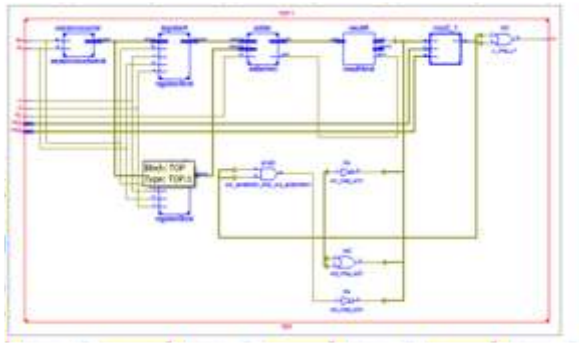


Figure3.6:Proposed RTL schematic

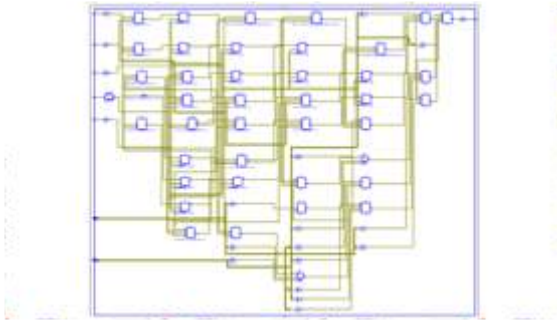


Figure3.7:Proposed tech.schematic

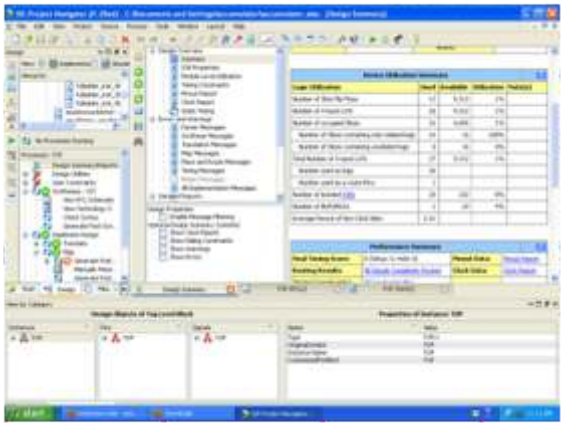


Figure3.8: Proposed device summary

Figure3.9: Proposed output wave when sel=0

Here clk, reset are used to set the register content. Given S=1,R=0 to set a flip flop. Here make selection line all zeros which makes the data from accumulator directly posed on CUT.No need to give input

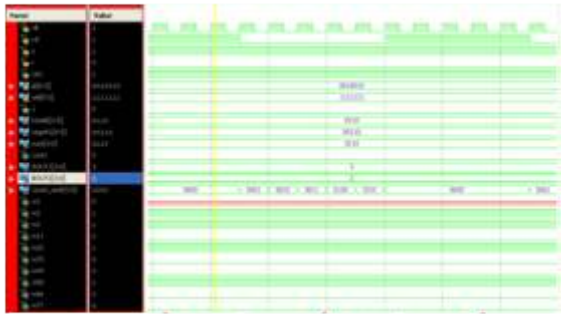


Figure3. 0 :Proposed output wave when sel=1

Here make selection line to all ones which makes the data from user directly posed on CUT.Need to give input,This input is given from a "Bus functional model".

V. CONCLUSION

In this work, a reliable ALU-based test pattern generation (0, 0.5, and 1)test-per-clock generation method, which can be used to effectively generate test patterns without modifying the layout of the adder is presented and verified by using SPARTAN 3E.

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