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Review of Contemporary Research in FinFET Technology

KEYWORDS: FinFET, LUT, Modeling, Physics.

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ABSTRACT As the scaling of MOSFET devices advances; Short Channel Effects (SCE) are being a dominant concern in microelectronics. In recent days, 3D multiple gate MOSFETs such as FinFET (Fin Field Effect Transistor) which possesses numerous advantages has attracted many researchers compared to conventional 2D planar MOSFETs. Major foundries have started using this technology in various scaling nodes. This document is a review of current research trends in FinFET technology and discusses its capability to change future of nano scale electronics. Various parametric advantages as well as issues with FinFET technology are discussed. Physics level design requirements for FinFET device modeling and logic design approaches are presented. Various mathematical models used to simulate the FinFET devices are reviewed. Recent replacement of planar MOSFET with FinFET in primary circuits of a complex design is discussed.

I. INTRODUCTION

As the MOSFET technology is being scaled down, new devices are required to be explored due to physical limitations of conventional MOSFETs such as significant increase in subthreshold leakage current (Ioff) with down scaling . This leakage increases the static power dissipation in off condition of device. As chips have millions of such devices, leakage current results in large power dissipation. The reason of higher off current is due to Drain Induced Barrier Lowering (DIBL) effect. To diminish this problem, gate-oxide thickness can be reduced but it leads to increase leakage due to Gate Induced Drain Leakage (GIDL) . To minimize GIDL, very high and abrupt drain doping is preferred because it provides lower series resistance as required for high transistor drive current . FinFETs (Vertical MOSFETs), one of the types of Multi-gate Field Effect Transistor (MGFET), are predicted as one of the best possible candidates to replace bulk MOSFET in the sub-45nm regime due to its improved subthreshold slope, reduced leakage current, better stability, higher (ION/IOFF) ratio, better short-channel performance, smaller intrinsic gate capacitance, and compatible process flow with existing CMOS technologies . Among various FinFETs, as per , Double gate FinFET transistors have finer SC characteristics and superior process variations protection. The reasons behind these advantages are 1.Use of thin silicon film, 2.Lightly doped channel and 3.Two gates for better channel control. FinFETs can be of following two major types: 1. Bulk FinFET in which fins and substrate share the common silicon area and 2. SOI - FinFETs in which silicon device is implemented on insulator. Two gates of the FinFET device are referred to as front-gate and back-gate and can be shorted together or driven independently, which classify it in a two major circuit types: Simultaneously Driven Double Gate (SDDG) FinFET circuits and Independently Driven Double Gate (IDDG) FinFET circuits. The back gate of the device can help to reduce the subthreshold conduction by applying higher voltage in case of PMOS and lower voltage in case of NMOS. The transconductance parameter, gm, can also be controlled by back gate bias. The difficulties arise with the FinFET technology is that, as reported in , FinFET structures experiences significant self-heating and the operating temperature in FinFET circuits varies directly with number of times the switching activity takes place. One more shortfall is that as the number of gates increases, the effective gate capacitance also increases. Figs.1(a)and1(b) show the various symbolic representation of double gate N-FinFET and P-FinFET respectively. Fig.2 shows the physical structure of FinFET showing the various regions. Various physical design considerations for FinFET are: 1. Fin Width, which determines the DIBL of device, 2. Fin Height, which is limited by the etching technology and 3. Fin Pitch, which ultimately decides the lay out area. As the number of Fins increases, device current capacity increases.

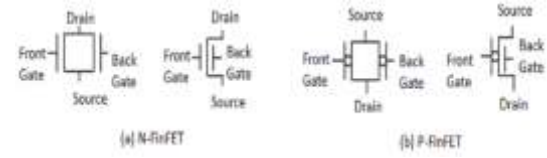

Fig. 1 FINFET symbols

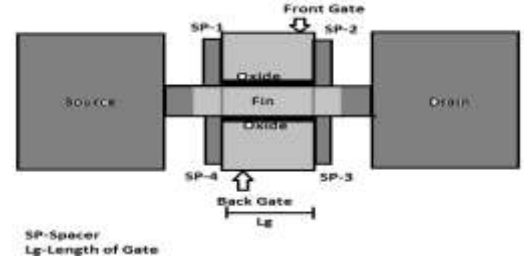

Fig. 2 FINFET structure

The paper is structured as follows. In Section II, brief information on double gate device physics along with Short Channel Effects (SCEs) are discussed. Different modeling methods for the simulations are briefed in Section III. Circuit/Logic design modifications are discussed in Section IV. Section V highlights the basic circuits which are currently being an interest of the researchers. Section VI summarizes the entire article.

II. FINFET DEVICE PHYSICS

FinFET is a nano-scale device. The following basic geometrical and physics parameters should be considered in modeling.

1) Natural Length and Current capacity

Natural length of single gate device can be found using

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equation (1) and for double-gate, it can be found using equation (2) . It clearly shows that the double gate device is two times thinner than the single-gate device and hence, device density can be increased for IC design.

$$\lambda_1 = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} t_{si}} \quad (1)$$

$$\lambda_2 = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{ox} t_{si}} \quad (2)$$

ε_{si}- silicon permittivity
ε_{ox}- Oxide permittivity
t_{ox}- Oxide thickness
t_{si}- Silicon fin thickness

Current capacity of double gate device is increased by the factor of number of gates used. It means that a double-gate device is capable to drive two times more current than a single gate device and hence, device can be ON in saturation swiftly. In FinFET, increase in number of fins or fin height helps to increase its current driving capacity. The problems faced while doing so is that more fins increase the width of MOSFET while more fin height faces difficulties in manufacturing process.

2) Short channel effects

A. DIBL and Punch-through

Due to short channel-length, depletion regions of drain and source are merged, this effect is known as the punch-through effect. For long channel devices, there is no direct effect of drain voltage electric field on to the channel ''' . However, for small devices, there is a strong impact of drain voltage onto channel which reduces the barrier potential and carriers can move through the channel even when gate voltage is much less than threshold voltage. Thus, gate loses its control on channel. This effect is known as Drain Induced Barrier Lowering (DIBL).

B. Surface Scattering

As the channel length is small, longitudinal electric field component Ey increases and surface mobility depends on field. Due to surface scattering, the mobility reduces to a great extent ''' .

C. Velocity saturation

At low electric field, velocity-field relationship is approximately linear ($v \approx \mu E$) which is maintained up to field value of 104 V/cm. After this value, velocity tends to increase very slowly compared to electric field and reaches to saturation value ''' . Due to velocity saturation, drain current get saturated at a lower drain voltage before channel pinch-off takes place. For low channel length devices, this effect is worth noticeable because before the onset of channel pinch-off, the carriers at the drain end get saturated.

D. Hot Electrons

Hot electrons generated due to high electric field can be trapped into oxide which increases the VTH and affect the control of gate on drain current.

III. FINFET MODELING APPROACHES

1.Physics-Core models of DG- FinFET

These models are purely based on physics of device and its parameters have the physical significance such as doping concentration, energy band etc. Physical models shows the specific phenomenon in transistor .

A. Surface Potential Model

3-D Poisson's equations are used to find the electronic potential in body.

$$\frac{d^2\Phi(x,y,z)}{dx^2} + \frac{d^2\Phi(x,y,z)}{dy^2} + \frac{d^2\Phi(x,y,z)}{dz^2} = \frac{qN_a}{\varepsilon_{si}} \quad (3)$$

It shows that electric field components in x, y and z directions is constant . In equation (3), q is the charge of electron and Na is acceptor concentration. Other physical effects such QME, SCE and PDE are included while considering the FinFET as short channel length devices.

B. I-V Model

Drift-diffusion equation can be used to obtain the I-V model. This model generates the drain current in terms of surface potential to obtain various device characteristics such as ID-VGS and ID-VDS.

C. C-V Model

For transient behavior of the device, I-V model is not sufficient which only describes DC behavior. Capacitance description is also needed. From the terminal charges of transistor, the intrinsic capacitance can be derived . These basic models are highly predictive and have high degree of accuracy. Simulation software such as TCAD uses these models in back-end part to show device behavior.

2. Empirical

This model is based on curve fitting. As per the measured data, it uses suitable equation to describe it. It can have exponents, coefficients, quadratic formulas, etc. Empirical modelling is curve fitting and parameters do not have any physical significance . As the device physics is becoming more and more complex, a pure physics based model is very much difficult to realize. Hence, combination of physics and empirical model proves to be sufficient modelling solution.

3. Look up Table(LUT)

Analytical models for FinFET devices are still under study and not available for circuit design. The LUT approach provides an attractive alternative for simulation of FinFET circuits since it does not required detailed physical description of device operation. In earlier MOS design, as the Channel length was more, subthreshold conduction was not a key issue, while for contemporary MOSFET designs it becomes a major issue because most of the transistors operate near sub-threshold region due to small supply voltage . LUT approach consists of I-V and Q-V tables, and interpolation coefficients for the transistor. This data is used to compute currents during circuit simulation . This approach overcome the difficulties of non-uniform grid and also addresses the important issue of representation of transition region. LUT approach is accurate for all three regimes and is efficient in terms of memory requirement and CPU time, and is robust.

A table based approach to study the impact of process variations such as channel length, fin width, and effective oxide thickness on FinFET circuit performance has been presented in . Steps to apply LUT-based approach were also shown. By interpolation method, large numbers of LUTs were generated. This interpolation method was also validated by comparing it with the TCAD simulated data. Three process parameters as discussed earlier were studied for different performance measures of circuits which include, time delay for buffer chain, static noise margin read and write for SRAM cell, and offset voltage, phase margin, gain, unity gain frequency for three stage op-amp. The shortfall of LUT is that there is a need to generate Q-V and I-V data from TCAD simulations then only table can be generated. To generate large number of data, interpolation is necessary in LUT approach.

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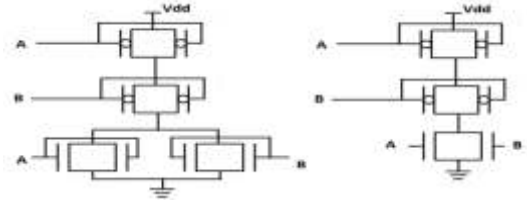
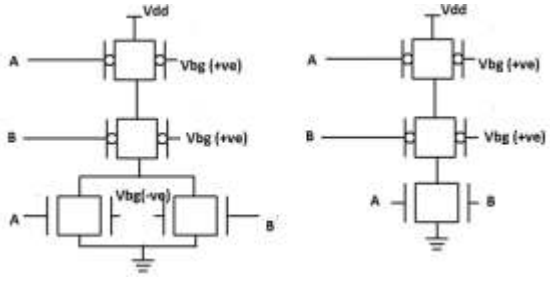
IV. CIRCUIT DESIGN APPROACHES FOR FINFET

For a double-gate FinFET, three configuration is identified: Shorted-gate (SG) mode with transistor gates tied together, low-power (LP) mode where the back-gate is tied to reverse-bias voltage to reduce leakage power, and independent gate (IG) mode where independent signals are used to drive the two gates of device . Combination of IG/LP-mode is also possible. In SG-mode, as both gates are tied together, FinFET functions as a planar MOSFET. IG-mode is helpful to control the Vth and gm of FinFET device. In Lower Power mode, back gates are connected to positive voltage for P-FinFET and to negative voltage for N-finFET which reduces the leakage and hence, subthreshold conduction. With all configurations, more advantageous DG/LP-mode is also presented in Fig.3 for NOR gate implementation using FinFET device.



(a) SG-Mode **(b) IG-Mode**

Fig.3(a) SG and IG-mode of operation for FinFET device



(c) LP-Mode **(d) IG/LP-Mode**

Fig.3(b) LP and IG/LP- mode of operation for FinFET device

It is reported in literature that DG-mode of operation proved to be the intermediate solution from the point of view of delay, leakage and Ion.

V. PRIMARY CIRCUITS: PLANAR MOSFET REPLACED WITH FINFET

In analog circuit design, FinFET is used to improve slew rate for op-amps and operational transconductance amplifiers (OTAs) as shown in . For digital circuits, it has shown various parametric advantages. In addition to various advantages of FinFET, substrate bias VBS was used to optimize sense margin and retention for 1T-DRAM cells . Using FinFET based technology, static noise margin enhancement of flex-pass-gate SRAM was discussed in''' . In , back gate bias technique of independently-gate devices was used to analyze the impact of spatial and temporal variations on stability of SRAM arrays. In , advantage of back gate is taken to design a low-noise, process-variation-tolerant sense amplifier. Intel and Samsung have started using FinFET technology at 22 and 14nm node respectively. Synopsys has delivered foundational modelling technologies for 3D circuit simulation, parasitic extraction and physical design-rule support of FinFETs.

VI. SUMMARY

In this review paper, we have studied the advantages of using FinFET compare to bulk planar MOSFETs. The basic physics parameters are also studied. Different modeling approaches for device design are shown. Circuit or logic designing approaches and their advantages are also discussed. Many research articles on FinFET are also referred in this study.

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