RESEARCH PAPER | Engineering | Volume - 5 | Issue - 1 | Jan Special Issue - 2015 | ISSN - 2249-555X



Review of Digital to Analog Converter

KEYWORDS: Binary weighted, Current steering, DAC, Segmented.

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ABSTRACT Scaling in CMOS technology becomes a great challenge to the analog designer as there are increases in design complexity with increase in shrinking. Digital-to-analog converters (DAC's) are one of the crucial modules of analog blocks facing high performance demand. In this paper first the traditional digital to analog conversion is discussed with circuit analysis. During the conversion process parameters are more important like resolution, SNR, SFDR which are discussed here. The performance of the DAC is measured by INL, DNL and quantization error which are also discussed. There are different types of DACs which are also discussed here using literatures. Some of these architectures are based on heuristic considerations. To understand the operations of DACs elementary studies are needed and after that it is possible to design optimum circuit of DACs. Furthermore, novel circuit strategies have been devised to deal with the challenge of reducing the power consumption, along with increasing the resolution and the frequency of process.

I. INTRODUCTION

The data available from real world are in analog form, but this analog data storage procedure is more complex compare digital storage. Following are more benefits of digital data storage: 1) digital data storage requires less memory compared to analog data 2) digital data are less noisy and 3) they provides excellent encryption and safety features. Thus in communication point of view we use analog to digital converter at transmitter side and digital to analog converter at receiver side. DAC is a useful building block in many-application because it represents the interface between the real world analog signal and the digital signal processors.

Fig.1 shows the data converter as interface in analog and digital domain. Transducers and sensors are used to convert the any form of energy in to the electrical energy. This electrical energy is analog data and using ADC we can convert the analog data in to the digital form using sampling and quantization. The access of electronics keen on areas like computers, communications, instrumentation and embedded systems such as mobile phones, i-phone, tablet, camcorders, HDTVs has given rise to call for DACs with stringent necessities [3].

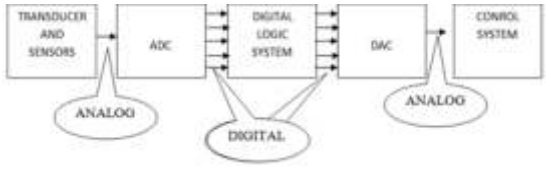

Fig. 1.Data converters as interface between analog and digital domain.[4]

II. BASIC DAC

Fig.2 shows the basic block diagram of digital to analog converter. Here N-bits digital data input is given to DAC and it converts into analog in form of voltage or current.

Here, an input N-bit digital word (b1, b2... bN) has a value Bin given by

$$Bin = b1 * 2^{-1} + b2 * 2^{-2} + \cdots + bN * 2^{-N} \ldots\ldots\ldots\ldots (1)$$

Where, bi is a binary digit, like 0 or 1. The bit b1 is the most significant bit (MSB) and bN is the least significant bit (LSB) [3].



Fig. 2.Basic digital to analog converter [3].

Output voltage Vout can be described by

$$vout = vref * Bin \ldots\ldots\ldots\ldots (2)$$

Where, v_{ref}= reference voltage. [3]

The digital input has a restricted amplitude resolution because of the limited word length or digit of bits. [5].

III. DAC PERFORMANCE

Dependent on purpose, different performance measures are used to describe the superiority and performance of a D/A converter [5]. There are two types of performance measurements: static and dynamic. Static properties are signal-independent (memory-less) and the dynamic properties are signal-dependent [5]. A classic static error is the divergence from the required straight-line input/output DC transfer characteristics, for example gain error, offset, differential nonlinearity (DNL) and integral nonlinearity (INL), etc. The dynamic errors mostly become more dominating as the signal and clock frequencies rise, while the static errors are dominating at lower frequencies. Dynamic performance is determined by signal-dependent errors such as slewing, clock feed through, glitches, settling errors, etc [5].

1. Static performance

A. Offset error

When zero digital code applied to the input, the difference between the ideal and actual DAC output is called offset error. Offset error occurs due to some leakage characteristic of the component which we used for designing DAC. Reduction in a leakage through the device will help to reduce offset error [5]. Offset error shown in fig.3.

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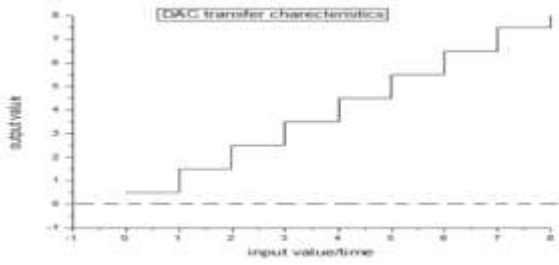

Fig. 3. Offset error in digital to analog converter.[5]

B.Gain error

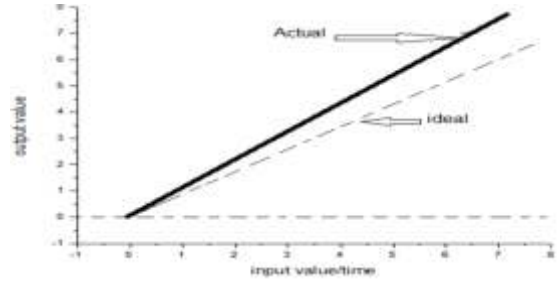

Fig. 4. Linear Gain error in digital to analog converter.[5]

When full scale digital code applied to input, the difference between the ideal and actual output is called gain error. Fig 4 shows the linear gain error. Compared with the ideal straight line (dashed), the actual line (solid) has a dissimilar slope in the linear or in the nonlinear. Linear gain error does not set up additional distortion as long as the signal is not extract. Nonlinear gain errors establish distortion as shown in fig 5. [5].

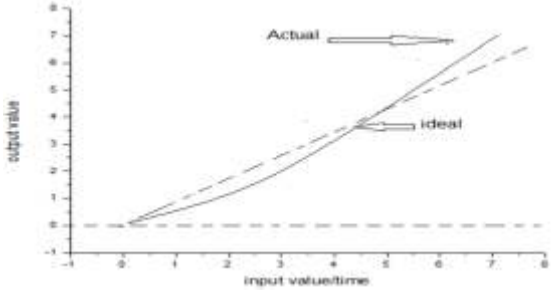

Fig. 5. Non-Linear Gain error in digital to analog converter.[5]

C. DNL and INL

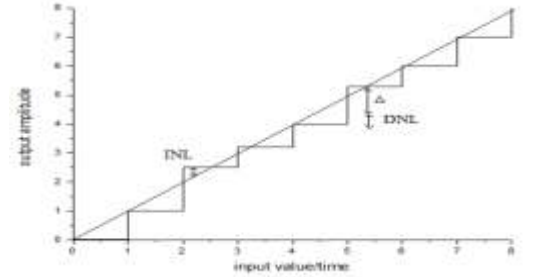

Fig. 6. INL and DNL in digital to analog converter.[5]

The INL state the variation from the straight line as shown in fig.6. DNL express how much variation in output level between two adjacent codes deviates from the ideal LSB step which is illustrated in fig.6. DNL describes the equality of the LSB sizes linking DAC codes. DNL represents the error in each step size, expressed in fractions of LSB. [5]

D.Monotonicity

If the output increases with an increase in input, we refer to this performance as monotonicity.[5]

2. Dynamic performance

A.Glitches

Glitches take place when the switching time instants of different bits in a DAC are matchless. This depend on matching errors in switches and driver circuits, time skew among switching signals, voltage-dependent CMOS switches, etc. For a small period of time fake code could come out at the output [5].

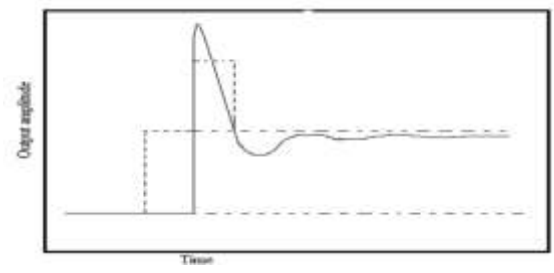

Fig. 7. Example of Glitch in digital to analog converter.[5]

B.Nonlinear settling

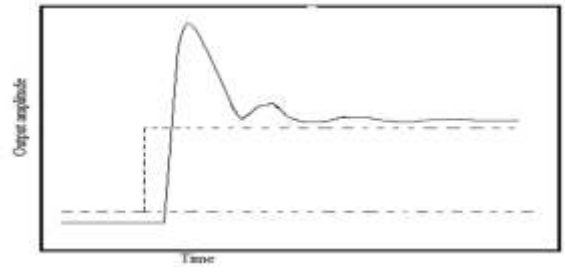

Fig. 8. Nonlinear settling in digital to analog converter.[5]

Fig.8 shows the "ideal" DAC output (dashed) and the actualDAC output (solid). When the input of the DAC is changed, the analog output should ideally change from the ideal start value, and settle towards the end value. In reality, the DAC cannot change its output value instantaneously; some degree of update time will source of settling error.[5]

C.Clock feed-through

There is a capacitance, c_{gs} or c_{gd}, between the digital switching signal and the sensitive analog signal. As a result of this capacitive coupling, or the Miller effect, in the switches, the clock (or digital switching signals) will affect the analog output signal. The CFT arises at both rising and falling edge of the switching signal. [5]

IV.FREQUENCY DOMAIN CHARACTERISTICS

1. HARMONIC DISTORTION

The power ratio of the xth harmonic and the fundamental is called harmonic distortion with respect to the xth harmonic

$$HD = 10\log_{10}\left(\frac{Px}{P1}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Where, P_1 is fundamental power and P_x is the power of xth harmonics.

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2.Total harmonics distortion
The ratio of the total harmonic distortion power and the power of the fundamental in an assured frequency band is called total harmonics distortion.

$$THD = 10\log_{10}\sum_{x=2}^{\infty}\left(\frac{Px}{P1}\right) \quad \ldots\ldots\ldots\ldots (4)$$

3.Signal to noise ratio
The ratio of the power of the fundamental and the total noise power within a certain frequency band, excluding the harmonic components is called signal to noise ratio.

$$SNR = 10\log_{10}\left(\frac{PS}{PN}\right) \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

Where, P_S is the signal power and P_N is the noise power.

4.Spurious-Free Dynamic Range
The ratio of the power of signal and the power of the largest spurious (unwanted) tone within a certain frequency band is called SFDR.

$$SFDR = 10\log_{10}\left(\frac{Ps}{Pk}\right) \ldots\ldots\ldots\ldots\ldots\ldots (6)$$

Where, P_S is the signal power and P_K is the spurious power.

V. DAC ARCHITECTURE
Digital-to-analog converters can be built via several different topologies. Each topology has a variety of strengths and weaknesses.

1.Voltage scaling DAC

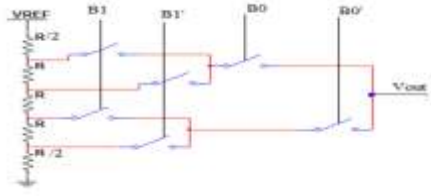

Fig. 9. 2-bits Voltage scaling digital to analog converter.[4]

Fig.9 shows a Voltage scaling DACs convert the reference voltage (Vref) to a set of 2^N voltages that are decoded to a distinct analog output by the input digital word. Voltage scaling selects sequence of resistors coupled between Vref and ground to achieve voltages between these boundaries. For N-bit converter, the resistor string would have at least 2^N segments. It is appropriate for MOS technology. A benefit of this structural design is that it guarantees monotonicity, as the voltage at each tap cannot be less than the tap below. The area required for the voltage scaling DAC is large, if the number of bits is greater than or equal to eight. Moreover, the switch rate of the converter will be sensitive to parasitic capacitances at each of its internal nodes.[4]

2. Charge scaling DAC

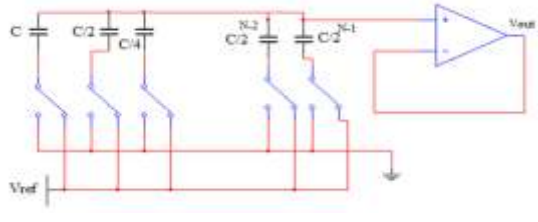

Fig. 10. Charge scaling digital to analog converter.[4]

Charge scaling DACs drive by dividing the total charge applied to a capacitor range in binary mode. This practice is implemented by using capacitors to attenuate the reference voltage as suggested by fig.10. This design is simple and purposes a digitally controlled voltage attenuator. This formation is precise, sensitive to parasitic capacitance, non monotonic and charge feed-through occurs at position on of switches.

3. Current scaling DAC
Current scaling DACs classically convert the reference voltage Vref, to set of binary weighted currents. The current are usually applied to an op-amp in the inverting terminal to form the analog output voltage, Vout.

$$vout = -Rf(I1 + I2 + \cdots\ldots\ldots\ldots\ldots + I(N-1)) \ldots\ldots\ldots (7)$$

A. Binary weighted resistor DAC

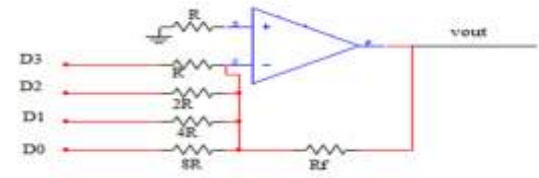

Fig. 11. Binary weighted resistor digital to analog converter.[4]

Fig.11 shows DAC using Binary weighted resistor. It is fast because here parasitic capacitors are not considered. But this DAC has constraint for resistors with a large value range.

B. R-2R ladder Binary weighted DAC
Fig.12 shows the R-2R Binary weighted DAC. The "ladder" name comes from the ladder like topology of the network. Here, the network consists of only two resistor values; R and 2R. No issue on, how many bits build up the ladder? Output errors due to resistor tolerances are habitually ignored in the design of the digital to analog conversion (DAC) circuit and in the selection of the R/2R ladder itself. It is simple and most accurate design with low cost compare to the Binary weighted DAC

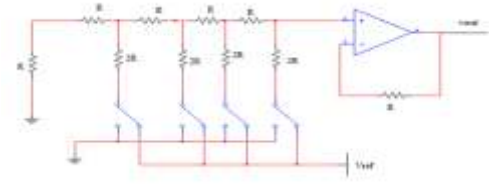

Fig. 12. R-2R ladder binary weighted digital to analog converter.[4]

4.Current steering DAC
Current steering has become most popular now a day due to its property to provide relatively huge currents (10 to 20mA) to 50Ω load without buffering. Moreover, speed of a current-steering converter is determined by the capability to drive the gates of the switches. Sample rates of several hundreds of millions of samples per second can be achieved. There are three types of current steering: Binary, Unary, Segmented

A. Binary weighted

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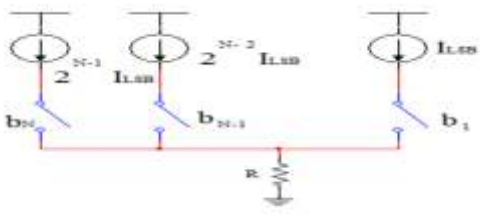

Fig. 13. Binary weighted digital to analog converter.[4]

Fig.13 shows Binary-weighted style uses current source in each branch to produce the analog signal. The value of the current source in nth branch is 2nI where I is the value of unit current source. Major advantage of binary-weighted DAC is its lesser area because it does not require any extra decoding circuitry.

Sadly, this arrangement does not guarantee monotonicity because sometimes by changing 1 LSB in the input code (for example from 011 to 100) the output can change more than 1 LSB (and for a short time it could be 111) due to this a large glitch energy. Furthermore, the glitch in binary-weighted is relative to the number of switches.[6]

B. Thermometer-decoded DAC(unary)

The equal amount of current in every branch is called "Unit-Element Array". In this structure, with 1 LSB alter in the input binary code just one additional current source is switched on or off depending on code change so it promises monotonicity. Another benefit of thermometer-decoded DAC over binary-weighted DAC is improved matching property of transistors. In binary-weighted the matching ratio is suitable to binary weights, and it must be almost exact value as several errors in matching is multiplied using binary weights. Finally, the third advantage is that the glitch is approximately zero, like in the binary-weighted is always relative to 1 LSB. The main weakness of thermometer-decoded DAC is that binary-to-thermometer decoder is needed; thus its area is larger than binary-weighted DAC and is not used for resolutions higher than 8 bits. [6]

C. Segmented DAC

Segmented DAC combine the rewards of both binary-weighted and thermometer-decoded structures jointly. In this technique, the input binary code is separated into 2 segments. In MSB segment where accuracy is significant, thermometer-coding is used. Binary-weighted structure is used in LSB segment to shrink the area of the chip. Occasionally, even these segments are separated into subsections and different strategies are used in each segment. This is called a "Multi-segmented" DAC [6].

TABLE I
COMPARISON CURRENT STEERING DAC STRUCTURE

Architecture	Binary	Unary	Segmented
INL	equal	Equal	equal
DNL	poor	Best	good
Glitch	poor	Best	good
Area	best	Poor	good
Power	best	Poor	good
Complexity	best	Poor	good

IV. SUMMARY

In this paper, we have the importance of Digital to analog converter and its different types. Each types of DAC have its own advantages and disadvantages. Depend on the application we can use any of them. These different methods are used as per the condition for the high speed, high resolution, less area, low power dissipation, low voltage etc. Now a day there is trends of high speed which is fulfill by segmented architecture.

REFERENCE

[1] SABYASACHI CHAKRABORTY," A critical Study on Digital to Analog Conversion and vice versa and introduction to Fuzzy circuit interface", International Journal of Scientific & Engineering Research, Volume 3, Issue 8, August-2012 ISSN 2229-5518. |[2] Jignesh B. Patel and Asst. Prof. Bhavesh H," Analog to Digital Converter (ADC) Review", IJETEE – ISSN: 2320-9569, Vol. 3, Issue. 2, May-2013. | [3] Anshul Agarwal," Design of Low Power 8-Bit Digital-to-Analog Converter with Good Voltage-Stability", May 2013. | [4] Pankhaniya shyamkumar amrutlal," study and implementation of high speed current steering digital to analog converter", may-2012. | [5] J Jacob Wikner," STUDIES ON CMOS DIGITAL TO-ANALOG CONVERTERS",2001.| [6] Peiman Aliparast, Ziaddin Daie Koozehkanai, Jafar Sobhi," Design of a 10-bit Low Power Current-Steering Digital-to-Analog Converter Based on a 4-D Thermometer Decoding Matrix", MIXDES 2010, 17th International Conference "Mixed Design of Integrated Circuits and Systems", June 24-26, 2010, Wrocaw, Poland. | [7] Soheil Radiom, Behzad Sheikholeslami, Hamed Aminzadeh, and Reza Lotfi, "Folded Current Steering DAC: An Approach to Low-Voltage High-Speed High-solution D/A Converters," 0-7803-9390-2/06 © 2006 IEEE. | [8] Guoyuan Fu, H. Alan Mantooth, and Jia Di, "A 12-Bit CMOS Current Steering D/A Converter with a Fully Differential Voltage Output," 978-1-61284-9140/11 © 2011 IEEE. | [9] Maruthi Chandrasekhar Bh, Dr. Sudeb Dasgupta," A 1.2 Volt, 90nm, 16-Bit Three Way Segmented Digital to Analog Converter (DAC) for Low Power Applications", 10th Int'l Symposium on Quality Electronic Design, 978-1-4244-2953-0/09/$25.00 ©2009 IEEE. | [10] LIN et al.," A 12-bit 40 nm DAC Achieving SFDR > 70 dB at 1.6 GS/s and IMD < –61dB at 2.8 GS/s With DEMDRZ Technique", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 3, MARCH 2014. | [11] Allen and holberg, "CMOS analog circuit design". | [12] Behzad razavi, "Design of analog CMOS Integrated circuits". | [13] R.Jacob Baker,"CMOS mixed signal circuit design".| [14] Rudy van de Plassche,"CMOS Integrated Analog-to-Digital and Digital –to-Analog Converters",2nd edition,Springer.