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Simulation of Multilevel Inverter with Reduced Number of Switches

KEYWORDS: DC/AC power conversion, multilevel multistring inverter.

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ABSTRACT Multilevel inverters have been developed to handle high power and high quality demanding applications. The objective of this paper to study five level multistring inverter topology for distributed energy resources (DER). High step up converter is used to boost and stabilize the output dc voltage of various DERs. This topology requires only six switches instead of eight required in conventional cascaded H bridge inverter. The studied multistring multilevel inverter offers strong advantages over conventional topology. Simulation of single phase inverter is done to verify result using PSIM.

I. INTRODUCTION

ultilevel inverters are emerging as effective solution for high power DC-AC conversion. Multilevel inverter that synthesized staircase voltage waveform from equally divided capacitor voltages with the help of appropriately connected power switches. Controlled switching of semiconductor switches plays a crucial role to achieve a multistep waveform with controllable amplitude, frequency and phase. Such an approach to DC–AC conversion offers a number of advantages over conventional two-level inverters, such as: capability to operate at higher voltages using traditional semiconductors, reduced dv/dt stresses, reduced common mode voltages, staircase waveform with better harmonic profile, smaller filter requirements and possibility of fault-tolerant operation.

The multilevel converter using cascaded-inverters is most promising for utility interface applications because of its capabilities of modularization and soft-switching. Conventional Cascaded H-Bridge (CCHB) five level inverter using 8 switches per phase leg shown in fig.1.

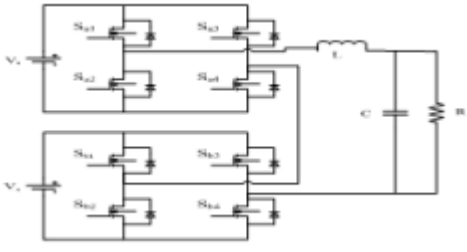

Fig.1. Five-level inverter topology of CCHB inverter.

In cascaded H-bridge inverter outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. Comparison of the power component requirements per phase leg among the three multilevel voltage source converters assumes that all devices have the same voltage rating, but not necessarily the same current rating, and that the cascaded-inverters type uses a full bridge in each level as compared to the half-bridge version used in the other two types.

TABLE I COMPARISON OF POWER COMPONENTS REQUIREMENT PER PHASE LEG AMONG THREE MULTILEVEL INVERTERS

Converter type	Diode Clamped	Flying capacitor	Cascaded H-Bridge
Switching devices	2 (m-1)	2 (m-1)	2 (m-1)
Clamping diodes	(m-1) (m-2)	0	0
Balancing Capacitor	0	(m-1) (m-2)/2	0
DC bus Capacitor	(m-1)	(m-1)	(m-1)/2

The objective of this paper is to study a newly constructed transformer less five level multistring inverter topology for DERs. The multistring multilevel inverter topology that requires only six switches instead of the eight required in the conventional cascaded H bridge (CCHB) multilevel inverter. Among them, two switches are operated at the line frequency and others are operated at high switching frequency PWM. As lower switching frequency usually means lower switching loss and higher efficiency. In this paper, a new multilevel inverter topology is studied with a very simple consideration: the structure should be such that it can synthesize all the additive and subtractive combinations of the input DC levels.

I. MULTISTRING FIVE LEVEL INVERTER TOPOLOGY

As conventional power generation causes environmental problems, so that renewable energy sources have become very popular and demanding. Solar and wind energy have advantage of being pollution free and decreasing maintenance cost. A general overview of multistring multilevel inverter for different types DER modules given in fig.2[8].

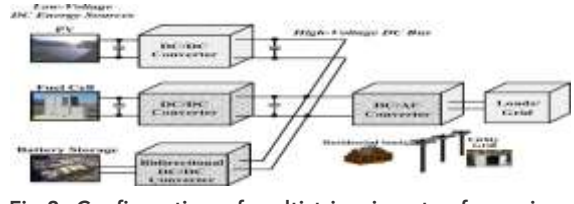

Fig.2. Configuration of multistring inverter for various DERs application[8].

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In this paper, the multistring approach is adopted because each dc–dc converter can independently perform. Another advantage of multistring configuration is that the mixing of different sources becomes possible, i.e., existing DER strings could be extended by adding new higher output panels without compromising the overall string reliability or performance. During installation and maintenance greater safety adds to the advantages of multistring configuration. Depending on the design, each converter module may be able to isolate its connected power source so that the wiring of series or parallel connection of these strings can be performed safely. The power-source-converter connection is a safe low-voltage connection.

The dc–dc boost converters are connected in parallel to avoid high dc-bus voltage, which will increase the size of the capacitors and the inverter's cost. Therefore, only two capacitors with equal capacitance rating are used as the dc bus, and the other dc–dc boost converters are connected to this dc bus, as shown in fig.2.

The single phase multistring multilevel inverter topology consists of two DER modules connected to their own dc to dc converter. Voltage balance is achieved by using DC bus capacitor for each individual high step up converter. Two capacitors are connected directly across the dc bus, assume $V_s1 = V_s2 = V_s$.

To obtain desired voltage level this topology uses six power switches, two fewer than the CCHB inverter with eight power switches. A comparison of presented topology with the classical topologies results in device count is significantly reduced for a given number of levels in the output.

III. PWM MODULATION

A number of modulation strategies are used in multilevel power conversion applications. The power levels of the inverter are largely restricted by carrier frequency. For air cooled design the frequency is practically limited to 3 to 5 KHz for large inverters, hence to increase power level it is proposed to operate two inverters in parallel with phase shifted carrier. The equivalent carrier frequency can be doubled and the output harmonics will be reduced. There are common two multicarrier based PWM methods.

PWM Algorithms for Multicarrier PWM Modulation:-

1) Phase Shifted (PS-PWM): Phase-shifted PWM (PSPWM) is a natural extension of traditional PWM techniques. A phase shift is introduced between the carrier signals of contiguous cells, producing a phase-shifted switching pattern between them. In this way, when connected together, a stepped multilevel waveform is originated. It has been demonstrated that the lowest distortion can be achieved when the phase shifts between carriers are 180° or $360^o/k$ for a CHB or FC converter, respectively. (where, k is the number of power cells).

2) Level Shifted (LS-PWM): Level-shifted PWM (LSPWM) is the natural extension of bipolar PWM for multilevel inverters. Each carrier is set between two voltage levels; hence the name level shifted.

Level shifted PWM technique is further categorized into three and they are: (i) Phase Disposition (PD):- They can be arranged in vertical shifts, with all the signals in phase with each other, called phase disposition. (ii) Phase Opposition Disposition (POD):- All the positive carriers in phase with each other and in opposite phase of the negative carriers, known as phase opposition disposition. (iii) Alternative Phase Opposition Disposition (APOD):- It obtained by alternating the phase between adjacent carriers.

A sinusoidal PWM is obtained by comparing a high frequency carrier signal with a low-frequency sinusoid signal, which is the modulating or reference signal. The carrier has a constant period; therefore, the switches have constant switching frequency. The switching instant is determined from the crossing of the carrier and the modulating signal.

This topology uses one reference signal and two carrier signals to generate PWM signals for switches. Both carrier signals Vcarr1 and Vcarr2 are identical to each other, except for an offset valueThe phase disposition PWM control scheme is introduce to generate switching signals and produce five output voltage levels: and $-2V_s0, V_S, 2V_S, -V_S$, .

IV. OPERATING PRINCIPLE

In this section, working principle of five level multistring inverter explained. The single-phase multistring multilevel inverter topology used in this study is shown in Fig. 3.

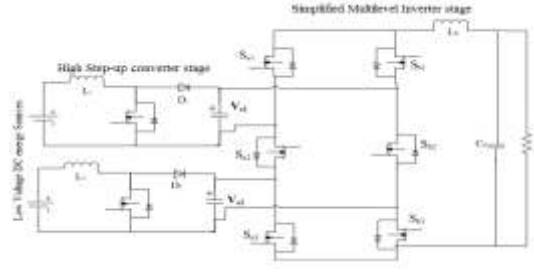

Fig.3. Single-phase multistring five-level inverter topology.

The corresponding operation modes of the multilevel inverter stage are described as follows[8].

1) Maximum positive output, $2V_S$: Active switches $Sa2$, $Sb1$, and $Sb3$ are ON; the voltage applied to the *LC* output filter is $2V_s$.

2) Half-level positive output, $+Vs$: This output condition can be induced by two different switching combinations. One switching combination is such that active switches $Sa2$, $Sb1$, and $S3$ are ON; the other is such that active switches $Sa2$, $Sa1$, and $Sb3$ are ON. During this operating stage, the voltage applied to the *LC* output filter is $+Vs$.

3) Zero output, 0: This output condition can be formed by either of the two switching structures. Once the left or right switching leg is ON, the load will be short-circuited, and the voltage applied to the load terminals is zero.

4) Half-level negative output, $-Vs$: This output condition can be induced by either of the two different switching combinations. One switching combination is such that active switches S_{a1} , S_{b2} , and S_{b3} are ON; the other is such that active switches S_{a3} , S_{b1} , and S_{b2} are ON.

5) Maximum negative output, $-2Vs$: During this stage, active Switches S_{a1}, S_{a3}, and S_{b2} are ON, and the voltage applied to the LC output filter is $-2Vs$.

As shown in below Fig. lists switching combinations that generate the corresponding operation mode of the five level inverter stage.

TABLE II SWITCHING COMBINATIONS

S_{a1}	S_{a2}	S_{a3}	S_{b1}	S_{b2}	S_{b3}	V_{AB}
0	1	0	1	0	1	$2V_s$
0	1	1	1	0	0	V_s
1	1	0	0	0	1	V_s
1	1	1	0	0	0	0
0	0	0	1	1	1	0
1	0	0	0	1	1	$-V_s$
0	0	1	1	1	0	$-V_s$
1	0	1	0	1	0	$-2V_s$

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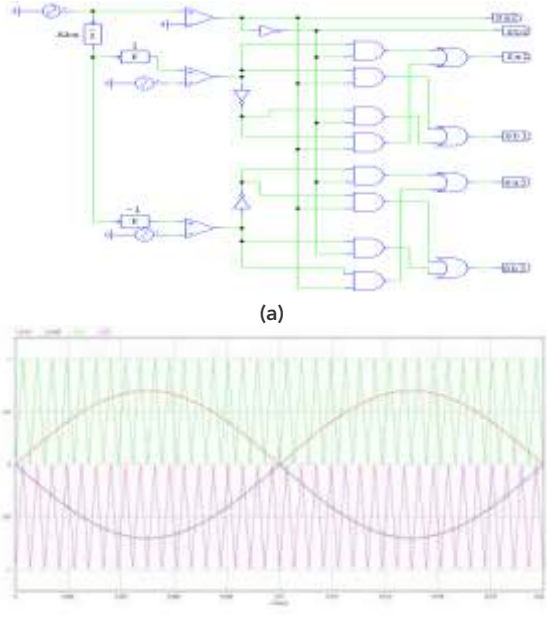
It can be observed that in this operation the open voltage stress of the active power switches S_{a1}, S_{b1} , S_{a3} and S_{b3} is equal to input voltage VS . The main active switches S_{a2} and S_{b2} are operated at the line frequency. Hence, this topology reduced resulting switching losses and overall efficiency is improved. If one of the DER is disconnected from the dc bus, the operation of the other dc–dc boost converters will not be affected because they are connected in parallel.

V. SIMULATION RESULTS

To verify feasibility of the single phase five level inverter, circuit is simulated using a widely used PSIM software. Switching instant is obtained by comparing a high frequency carrier signal with a low-frequency sinusoid signal. Both V_{tri1} and V_{tri2} are carrier signals compare with sinusoidal signal. The peak to peak value of the triangular modulation signal is 1 and switching frequency is 1.8 kHz for both carrier signals. The peak value of sinusoidal modulation signal is taken as 0.7 and frequency, f_m=50 Hz. According to this modulation scheme, modulation logic and carrier/reference signal is shown in fig.4. Input sources, DER module 1, and DER module 2 of 30V are connected to the inverter followed a linear resistive load through the high step-up dc/dc converters. The input voltage is feeding from two high step up converter at 150V, i.e. $V_{s1} = V_{s2} = V_s$.



(a)

(b)

Fig.4. Modulation strategy: (a) modulation logic (b) carrier/reference signals.

To solve problem of complex control circuits for conventional multilevel inverters, single-phase multistring topology, presented as a new basic circuit in Fig. 5.

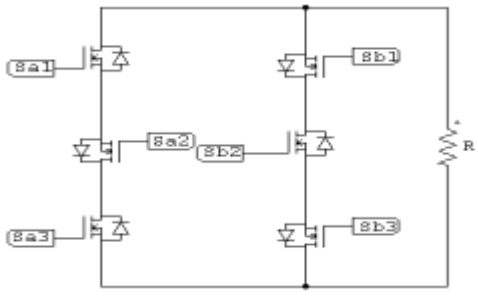


Fig.5. Five level Inverter Circuit with reduced number of switches.

This paper uses multicarrier phase disposition modulation technique to generate the modulating signals for the inverter switches. It can be a useful solution for pulse generation for this topology. This distributed of switching frequency amongst switches is extremely significant because they bear different voltage stresses. As S_{a1}, S_{a3}, S_{b1} and S_{b3} operate at high switching frequency, they bear a stress of 100V each. Switches S_{a2} and S_{b2} which bear the highest voltage stress of 200V each, commutate at frequency of 50 Hz. The switch voltages of S_{a1}, S_{a2}, S_{a3}, S_{b1}, S_{b2} and S_{b3} are all shown in Fig.6.

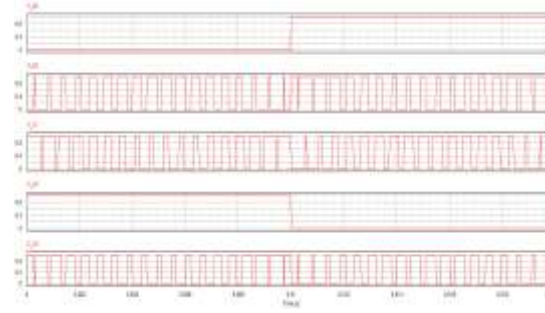


Fig.6. Simulated waveforms of switch voltage for inverter stage.

For verifying the validity of the studied multilevel inverter in the generation of a desired output voltage waveform, simulation is done according to the modulation logic that shown in Fig. 4(a). The multilevel shown in Fig. 7 is adjusted to produce a 50-Hz, 5-level staircase waveform for a resistive load of 50Ω. The simulated waveform of the phase voltage with five levels is shown in Fig.7.

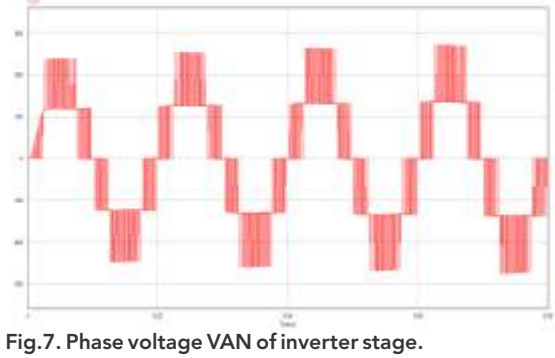


Fig.7. Phase voltage VAN of inverter stage.

As far as comparison of the CCHB and studied multilevel inverter topology is concerned, this studied multilevel inverter have lower THD than the CCHB multilevel inverter.

TABLE III
COMPARISON OF TWO MULTILEVEL INVERTER

Inverter type	CCHB Inverter	Studied Multilevel Inverter
Number of Switches	8	6
Voltage stress	S_{a1}-S_{a4}: V_s S_{b1}-S_{b4}: V_s	S_{a1}, S_{a3}, S_{b1}, S_{b3}: V_s S_{a2}, S_{b2} : $2V_s$
%THD (V_{AN})	0.43	0.27

It implies that the output waveform is improved and smaller filter size can be used.

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VI. CONCLUSION

This paper presents a single-phase multistring five-level inverter for DER application. This topology reduces number of power devices for a given number of levels in the output. The circuit topology, control algorithm and operating principle of the multistring multilevel inverter have been analyzed and simulated using PSIM. Simulation result shows that studied topology reduce THD, smaller filter size and improved output waveform compared to classic topology.

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