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Research Paper

Engineering

Routing Packets On A Chip : Network On Chip Algorithm

* Naren V Tikare

* Dept. of Electronics and Communication, Bapuji Institute of Engg. and Tech., Visvesvaraya Technological University, Karnataka

ABSTRACT

In this paper, static method of routing packets is proposed for a Network-on-chip. Network-on-chip is a collection of several nodes connected together in a closed loop. Every node in the Network-on-chip has its unique addresses which help to establish communication between desired intellectual properties. In order to prevail static routing, all the nodes in the Network-on-chip consists of a CAM routing table. The table holds the addresses of all the nodes in the Network-on-Chip. The connection is established by a special packet called route establishing packet. This packet holds the addresses of the source and destination nodes. As this packet traverses through various nodes, it links these two addresses in the routing table by a unique binary nibble. The data packet compares its nibble with the nibble in every node to which the source and destination address is linked. The node in turn will provide information about the destination of the packet. Hence, at the end of data transfer, route destruction packet delinks the two addresses in the routing table.

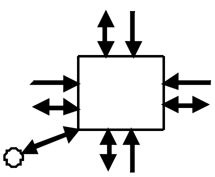
Keywords : Network, on chip networking, static routing, Network on chip.

Introduction

Network-on-chip is an emerging paradigm for communication, built on chip, for complex System-on-Chip architectures. It uses packet-switching for communication allowing integration of a large number of computational, processing as well as storage blocks on a single chip. Network-on-Chips are aimed to provide enhanced performance, modularity, design productivity when compared to traditional communication architectures such as dedicated signal wires and bus architectures. In order to manage the vast number of transistors on chip, we will have to make use of some new technology arrangement, and for this virtue, SoC and NoC are the two main implementation approaches (Micheli, 2006). Presently, portable computers and cell phones and numerous products all implemented on a silicon chip (Smith) are all lively examples of SoC architectures. Due to ever increasing number of transistors (Smith) they will have a complex design and also long time to market as described in (L. Benini, 2007), (Widjaja, 2001), and (Benini, 2004). NoC provides efficient communication (The 2nd IEEE International Symposium on Networks-on-Chip, 2008) between all the cores in a SoC as in (L. Benini, 2007), (Widjaja, 2001), (Benini, 2004). The communication takes place by the help of packets where every packet takes a specific route within NoC for efficient communication between two IP's as discussed in (Special issue on networks on chip, 2004).

Architecture

Fig 1. Structure of a node



Information provider

Bi-Directional bus

Control bus

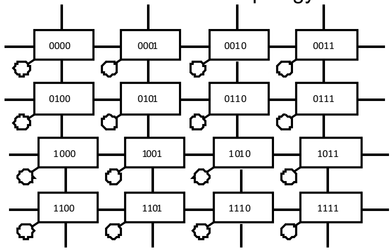
This is a simple node architecture as in (Special issue on networks on chip, 2004) which consists of

1. Bi-Directional buses
2. Control signals
3. Information provider (IPr)

All packets used in the network are 16 bit in size and are not variable in length. This allows the busses to be of 16 bits size and parallel bus architecture is faster and more reliable. The control signals used in this design help in proper communication between nodes, before and after packet transfer. The two control signals used are Request and Enable and are 1 bit in size. The control signals along with the busses are connected from every node to its neighboring node in all the directions.

Control signals used are hand shake signals which help in reducing traffic of packets in the network. Whenever a packet wants to travel from its current node, it requests for the availability resources to the next node to which it is to hop. If the node is not handling any other packet transfer, it acknowledges by Enable signal and thus the packet can initiate its move to the next node. Till the time, a packet is in a node, the node does not perform any other function other than processing the current packet and forwarding it to the next node. Once the processing is complete, and all resources are free, it is when it handles the next packet.

Fig 2. Architecture of NoC in Mesh topology



Methodology

NoC is a collection of several nodes connected together, as per design requirements and the efficiency of communication necessary. There are various different types of topologies, used for connecting the nodes in the NoC.

- Mesh (J. Duato, 2002)
- Torus (W.J. Dally C. S., 1986), Star (Micheli, 2006)
- Octagon (S. B. Akers, 1989)
- SPIN (Adriahantenaina, 2003)

Every node in the NoC consists of a bidirectional data bus for the flow of packets in and out of the node, control bus for handshaking between two nodes, placed at the outer jacket of the node. Every node is connected to the other node by these data busses and control signals. Every node connected, is given a unique address for its identity. The address may start from 0000 to 1111 for a combination of 24 nodes and from 00000000 to 11111111 for a combination of 28 nodes. There is a complex internal architecture in a node, consisting of a CAM routing table, and a buffer. CAM table consist of information like the addresses of all nodes in a NoC, with some free space to add some Additional Information (AI).

To initiate, an IP forwards a packet to the node connected to it in a NoC, hence, the packet hops across various nodes, till it reaches its destination IP. For subsequent routing of packets in the NoC, 3 types of packets have been introduced. They are:

- Route establishment packet (REP).
- Data packet (DP).
- Route destruction packet (RDP).

Firstly, REP is introduced into the network where it consists of just the payload and no header. Payload consists of

- Source and destination IP addresses.
- AI (nibble).
- Information about the number of hops (decrement counter).
- Direction bits provide information regarding the route within the network to reach the destination.

Fig 3. Route Establishing Packet

Direction bits	Number of hops	AI	Source and destination addresses

Suppose there is a need for data transfer between any two IP's, the source IP introduces a REP in to the network through the data bus connected between it and its corresponding node. The address of source and destination in REP is compared with that of CAM table. Once the addresses are found, they are locked together with a combination of 4 bits called AI. Once the packet is hopped from one node to another, the direction bits are shifted two bits left and hop bits are decremented by two. Hence, the remaining direction and hop bits are stored in the corresponding memory relating to AI. Direction bits provide information regarding the next node to be hopped in the network. Every move of the packet corresponds to two direction bits.

If 00= packet is moved left

01=packet is moved straight

10=packet is moved right

11=packet is returned to its previous node.

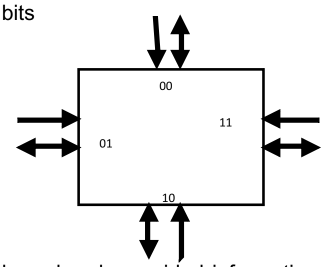
Hop bits are used as a down counter which is initialized at the beginning and reset to zero when the packet reaches its destination.

Thus in every node where REP flows, it leaves behind information regarding the destination address, number of hops and the path necessary for the forthcoming DP to track its destination.

The packet following REP is DP; it has a very small header and a large payload. The header just consists of

- AI (nibble)
- Data information.

Fig 4. Example showing forwarding of packets with respect to direction bits



As REP has already provided information to various nodes about the destination of the packet, DP just has to verify its AI with that of the information in the CAM, and it provides information about the destination, information of the next node and the number of hops needed by DP to the destination. Accordingly, DP is introduced by the source IP with just four bits of information and data.

Fig 5. Data Packet

Data	AI

When there are no more data packets to be transmitted from that particular source IP to the destination IP, the locked addresses in the CAM of a few selected nodes can be unlocked by the aid of transmitting a RDP from the source IP to destination IP, by transmitting it through the same nodes via which REP and DP were transmitted in prior. RDP consists of even less information when compared to REP and DP. The need of source and destination address is not necessary when transmitting RDP. Rather it may include the last bits of data as that of data packet in the payload and AI and number of hops in the header of RDP. When RDP enters the first node, it gathers information of the next node and deletes AI and its associated information about direction and the number of hops in the node. As it reaches the destination IP, it conveys the last packet of data and thus frees all locked nodes in the NoC for future communication.

Fig 6. Route Destruction Packet

Data bits	Zero bits	AI

Tools/ Implementation

The design of NoC is carried out in a software tool named Xilinx version 13.2. The simulation results have all been observed in simulation software called Modelsim. Firstly, the design is tested with various test benches, with at least more than thousand sets of input data. Input data corresponds to the three types of packets where the bits in the packet have been manually entered in the test bench as inputs, then the program is compiled and the corresponding simulation result is been observed. Once the design is working efficiently, it is then implemented in an FPGA, named Spartan 3. The design is well sophisticated with 980000 gates approximately. The specifications of the FPGA are given in (http://uk.farnell.com/xilinx/xc3s1500-4fgg456c/fpga-spartan-3-1-5m-gates-456fbga/dp/1762476).

Conclusions

NoCs are the emerging network solutions for SoC designs and have also tackled many disadvantages of SoCs. The design described in this paper focuses on the algorithm to route packets in the network by static means. It deeply discusses static methods to transfer packets between different IPs. The concept is well described by using 3 different types of packets namely REP, DP and RDP. Every IP connected to the NoC is given a unique address, which is saved in CAM routing table of all the nodes in NoC. When there is a need for data transfer from an IP to another IP connected to the same NoC, the source IP introduces REP in to the network, followed by DP; when the data is fully transmitted, source IP sends RDP and the connection between source IP and destination IP is erased.

There is a possibility that one NoC can be connected to another NoC; only if the design considerations such as bus width, control signals match each other.

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