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Software Defined GSM Baseband Processor in FPGA for Telemedicine Applications

KEYWORDS: FPGA, GSM, Telemedicine

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ABSTRACT *The structure of telemedicine system consists of communication modules like zigbee, GSM, Internet, WAN, PAN etc. to transmit the acquired bio-signals from the patient or remote centre to the experts for analysis. Hence a wireless communication becomes an essential in a telemedicine application. This paper describes the implementation of a GSM baseband processor on an FPGA that well suits for any telemedicine application. A programmable solution for a hardwired logic targeted on a reconfigurable architecture will definitely make the telemedicine system less complex. The proposed implementation has the advantage that various blocks of the processor can be reconfigured to support multiple signal processing tasks and also can be retargeted to any family of FPGA device.*

INTRODUCTION

Health care services at rural or remote areas can be definitely improved if the experts medical care are available promptly. Wireless technology and telemedicine has provided a new way in the delivery of health care. The ubiquitous nature of cellular network has provided a new way in telemedicine. Transmission of biomedical signal using wireless technologies has been the recent research in telemedicine.

One of the crucial cases where effective emergency telemedicine required is Coronary artery diseases because still two thirds of all patients die before reaching the hospital. According to a study [1] in the UK in 1998, it is seen that among patient above 55 years old, who die from cardiac arrest, about 91% die outside hospital, due to a lack of immediate treatment. In case of acute myocardial infarction the survival is related to the "call to needle" time, which should be less than 60 minutes [2].Therefore time becomes an essential factor for the acute treatment of heart attack or sudden cardiac death. ICT (Information and Communication Technology) plays an important role in creating versatile and cost effective alternatives to health care delivery. The performance of GSM and GPRS system in the transmission/reception of X-ray images and video in emergency orthopedics cases was discussed by S.Ch. Voskasides et.al[3].A test bed for telemedicine application on 3G cellular standard was proposed by SG. Miaou[4]. Hamid Noori et. Al has suggested a hardware DSP core using FPGA for speech coding applications [5].An implementation of GMSK modulator for GSM system on FPGA was discussed by Nitin Babu and Vinayakmurthi.K.K.[6].In the design context for wireless systems, the FPGAs are considered a good implementation approach because many of the digital signal processing tasks can be executed in parallel[7].

If the hardware components needed for the system operations are defined in terms of software components with standard interconnections, then the reliability of the overall system can be enhanced [8]. Thus, this paper proposes an implementation of a GSM modem as software component using FPGA.

GSM UPLINK IN FPGA

Global System for mobile communication (GSM) standardized by European telecommunication standard Institute has evolved as one of the most popular ICT in recent days. Commercial service of GSM has begun in the year 1991. From then onwards, the terrestrial and satellite network has grown to cover the whole world. The operation of frequency of GSM was originally 900 MHz and then adapted or changed to 1800 MHz and today it is brought down to 450 MHz.GSM not only transmits and receives speech signal but also provides variety of services like FAX, SMS and multimedia transfer. GSM, a circuit switching data network has a maximum data rate of 9.6kbps and later extended to 14.4 to 115.2 kbps and in future data rate of 384kbps per user might evolve.

Now-days a sophisticated system that provides voice, high bit rate, video, image and multimedia capability are the demands of the customer. To meet the above requirements a highly flexible system that can adapt to new models and signal processing techniques are needed. Telecommunication and network equipments like wireless stations, switches, routers, modems etc. finds its way into FPGA because of greater performance, economically less cost , flexibility and low power consumption of FPGA devices.

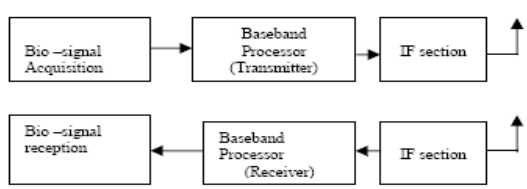

Figure 1: Structure of Telemedicine

Figure.1 shows a very simple block diagram of structure of telemedicine. Bio signals are acquired in the patient side and transmitted to the analysis centre through wireless medium. This paper aims in designing the baseband processor of GSM modem at the transmitter and receiver side on a reconfigurable platform that has low cost and high speed.

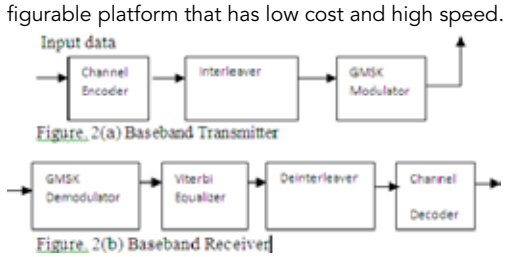

Figure 2(a) and 2(b) shows the blocks implemented on FPGA. Nitin Babu and Vinayakmurthi[7] has discussed the implementation of GMSK modulator on FPGA. The present work

Volume : 3 | Issue : 8 | Aug 2013 | ISSN - 2249-555X

discusses on implementation of signal encoding/Decoding, channel encoding/Decoding, Interleaver/Deinterleaver, GMSK Modulator/demodulator on FPGA.

CHANNEL ENCODER

Redundancy in data is introduced in channel coder for detecting and correcting errors that might occur during transmission. The 260 bit input to the convolutional encoder is divided into class Ia containing 50 bits , class II a containing 132 bits and class II with 78 bits. The class Ia bits are cyclic encoded using linear feedback shift register. The proposed work uses three registers to include 3 bits with 50 bit input pattern.Figure.3 shows the implementation of cyclic encoder for class Ia bits.As shown in Figure.3 class Ia 50 bit data is fed to the cyclic encoder. Since the required bit pattern is of the form (53,50), the generator polynomial used in this encoding process is $x^3 + x + 1$.

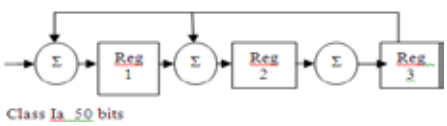

Figure .3. (53, 50)Cyclic Encoder

Once the 50 bits are completely shifted the content of register 1 to 3 contains the three redundant bits which is added to the 50 bit input data to generate 53 bits. The generated 53 bit data is added with 132 class Ib plus 4 extra bits to form 189 bits. Next stage of Convolutional encoding is to generate two bits for every input data. The output of the previous stage containing 189 bits is doubled to 378 bits. Convolutional encoder has been designed using the polynomial $G_1(x) = x^4 + x^3 + 1$ and $G_2(x) = x^4 + x^3 + x + 1$. The output of the convolutional encoder is 378 bits which is further added with class II 78 bits to generate the final 456 bits which is fed to the interleaver, next stage of GSM transmitter.

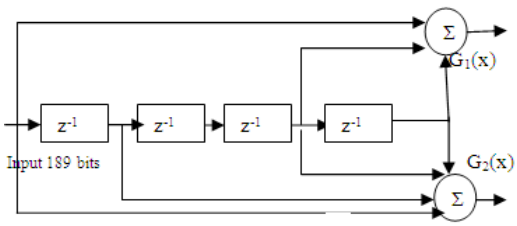

Figure.4. (378,189) Convolutional Encoder

INTERLEAVER /DEINTERLEAVER

Fading is always one of the major impairment in RF channel that results in errors in consecutive bit patterns. Interleaver arranges the code word symbols in such a way that errors are spread among multiple code words. The output of the convolutional encoder is divided into 8 blocks with each block containing 57 bits as shown in Table.1.

Table 1.
OUTPUT OF INTERLEAVER

Output of the convolutional encoder	0	1	2	3	----------	456	Final Read out
I Block	0	8	16	24	----------	448	
II Block	1	9	17	25	----------	449	Even bits
III Block	2	10	18	26	----------	450	
IV Block	3	11	19	27	----------	451	
V Block	4	12	20	28	----------	452	
VI Block	5	13	21	29	----------	453	Odd Bits
VII Block	6	14	22	30	----------	454	
VIII Block	7	15	23	31	----------	455	

The first block is formed by taking every 8^{th} bit that is selecting the 0^{th} , 8^{th} , 16^{th} bits and so on. Similarly, the second block is formed by taking the 1^{st}, 9^{th} ,17^{th} bit and so on. The same procedure is repeated to form the 8 blocks. The bits in the first four blocks occupy the even positions and the bits in the next 4 blocks are placed in the odd position for a total of 456 bits.

GMSK MODULATOR

An extension of Minimum shift keying (MSK) is Gaussian Minimum Shift keying (GMSK), a continuous phase modulation scheme.

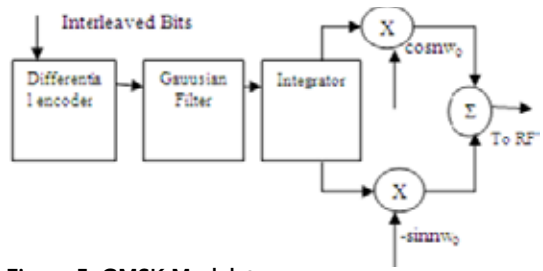

Figure 5. GMSK Modulator

Initial step in GMSK modulation is differential encoding that is incoming binary sequence is expressed in (Non Return to zero) NRZ format followed by convolution with a Gaussian function that meets the following specifications: a function with narrow bandwidth and sharp cut off frequency and a small overshoot impulse response to avoid excess deviation. The bandwidth time product to design the filter has been chosen as 0.3, as per GSM standard. The impulse response of the Gaussian filter is given by

$$h(t) = \frac{1}{\sqrt{2\Pi}\sigma T} e^{-t^2/2\sigma^2 T^2} \quad ----(1)$$

where

$$\sigma = \frac{\sqrt{\ln(2)}}{2\Pi BT} \quad ----------(2)$$

$$BT = 0.3$$

The resulting signal is integrated and then multiplied with carrier signal represented by $\cos n\omega_0$ and - $\sin n\omega_0$ to generate inphase component (I) and quadrature phase component (Q) respectively. Then the two signals (I & Q) are summed up to generate the resultant signal. The reason to prefer GMSK modulation in GSM is that the information to be transmitted is contained in phase variation rather than amplitude. This leads to higher signal to noise ratio i.e the signal is more immune to noise. And also, a non linear amplifier that consumes less power can be used at the receiver to demodulate the signal leading to low battery usage an essential performance criteria in cellular technology. The output of the modulator feeds the RF circuit for transmission.

GSM DOWNLINK IN FPGA

The various blocks of GMSK coherent Demodulator are shown in Figure 6. The GMSK modulated signal is allowed to pass through a band pass filter and then multiplied with the carriers $\cos nw_0$ and $-\sin nw_0$.

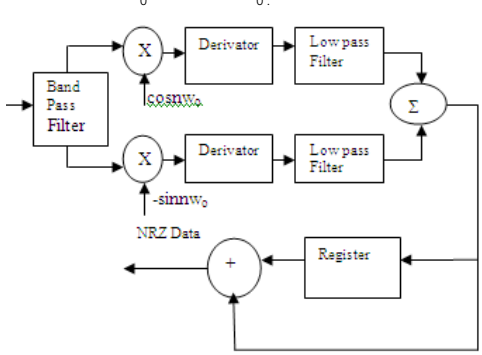

Figure 6. GMSK Demodulator

Volume : 3 | Issue : 8 | Aug 2013 | ISSN - 2249-555X

The derived resultant signal is low pass filtered to recover the inphase and quadrature phase component and then added . To retrieve the differentially encoded bits a modulo -2 – addition is performed.

VITERBI EQUALIZER

Performance of the receiver can be improved by using an equalizer which mitigates inter symbol interference (ISI) and to overcome the fading due to multipath propagation.

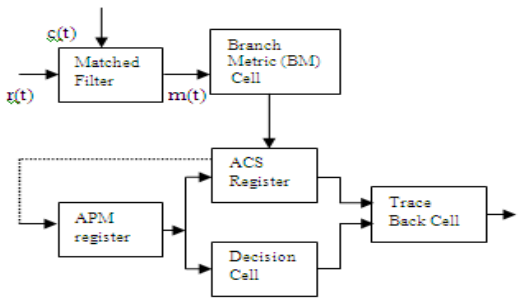

Figure 7. Viterbi Equalizer

The implementation of Viterbi equalizer with matched filter and various registers to compute the transmitted bits are shown in Figure 7. The coefficients of matched filter have been computed by cross correlating the received sequence with a trained binary sequence. The output of the matched filter drives a Branch metric cell which calculates the metric by using squared Euclidean distance. Accumulated path metric(APM) register summarizes the branch metrics and this register has been updated by the selected path by add compare and select(ACS) register. A trace back unit finally decodes the bits.

DEINTERLEAVER

Deinterleaving is the reverse process of interleaving. During interleaving the 456 bits are stored in SRAM that consists of 8 rows and 57 columns. Fig 7. shows the write cycle of the interleaver in which every 8th bit is stored row wise. SRAM for deinterleaving process consists of 57 rows and 8 columns. As the data enters, it is written in column wise as shown in Figure.8 and during the read cycle the bits are read row wise which accomplishes the deinterleaving process as shown in Figure.9

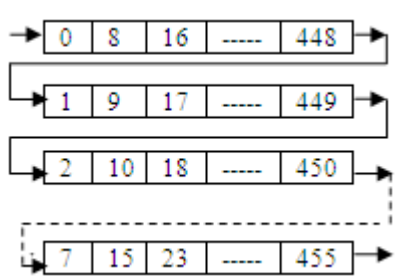

Figure 7 . Read cycle of Interleaver

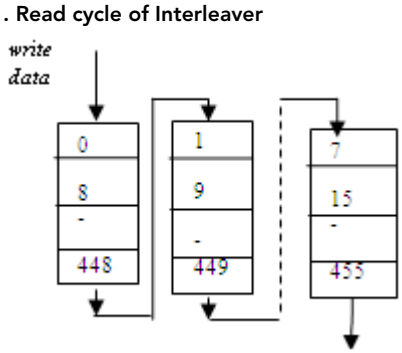

Fig.8 . Write cycle of Deinterleaver

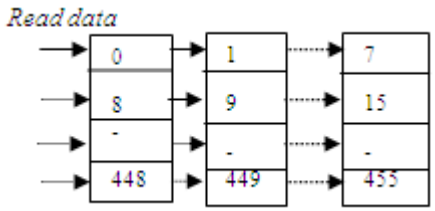

Fig.9 . Read cycle of Deinterleaver

CHANNEL DECODER

A hard decision Viterbi decoder has been implemented to get back the data transmitted. The working of Viterbi decoder cab be best explained by the flowchart shown in figure.10. Branch metric has been calculated using the hamming distance between the received pairs and ideal pairs. Add –Compare –Select has been used to determine the path metric. New path metric is calculated by adding the previous path metric with corresponding branch metrics. Then the path with greater metric is dropped and the path with least metric is selected. During decoding process, memory and temporary registers are used for storing the various parameters and path metrics.

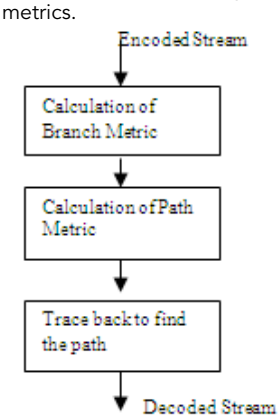

Figure.10 . Flowchart for Viterbi Decoder

IMPLEMENTATION AND RESULTS

The proposed work has been implemented in programmable logic device design software Quartus. Verilog codes for various blocks of uplink and downlink process are modeled and implemented in cyclone IV kit . RTL schematic for uplink and downlink process is shown Figure.12 and Figure.13. Implemented blocks were simulated and its corresponding timing diagram obtained is shown in Fig.14. The result as shown in Figure.11 indicates that 49 logic elements(LE's) were utilized out of 22,320 LE's which is less than 1% utilization. The implementation of this module clearly reveals that complex applications can be built in parallel with GSM baseband processor on the same FPGA. Thus, a Telecardiac system can be implemented with acquisition , analysis and transmission of bio signals using a single FPGA . Thus the implemented work can be extended to design a portable system with real time acquisition and processing of ECG signals on the patient side and alarm the doctor or caretaker about the condition of the patient.

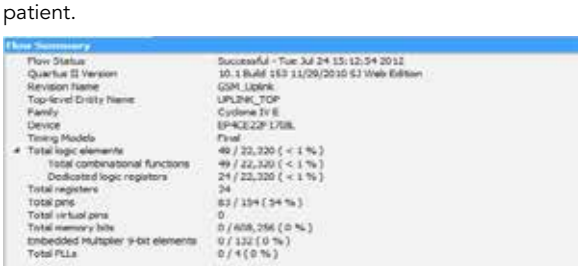

Figure. 11. Utilization summary

Volume : 3 | Issue : 8 | Aug 2013 | ISSN - 2249-555X

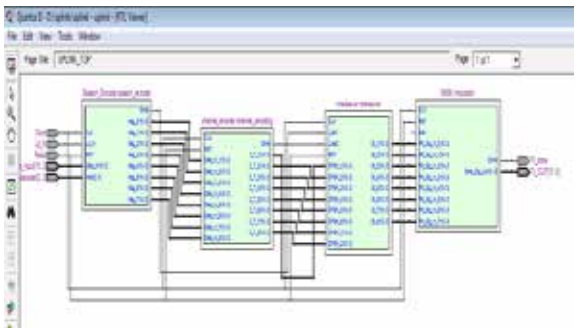

Figure.12 . RTL Schematic of GSM Uplink

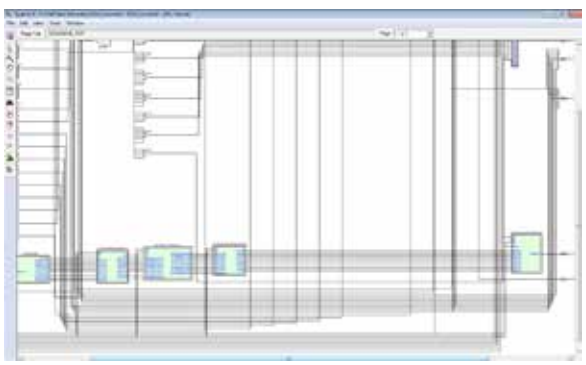

Figure 13 RTL Schematic of GSM Downlink

CONCLUSION

This paper discusses on implementation of software defined GSM baseband processor in a FPGA. This can be further integrated with a real time healthcare monitoring and processing application like ECG or EEG that runs on the same FPGA board . Thus this implementation enhances the process involved in telemedicine.

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