RESEARCH PAPER | Engineering | Volume : 3 | Issue : 8 | Aug 2013 | ISSN - 2249-555X

CMOS Band Gap Reference (BGR) Design Techniques: A Review

KEYWORDS: Low-voltage, CMOS Bandgap Reference (BGR), Ultra Low Power, Deep submicron

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ABSTRACT *As the CMOS technology has developed rapidly during the past several decades and has brought us into a new era of high integration and ultra–low power consumption circuits. Shrinking device dimensions in advancing CMOS technologies require lower supply voltages to ensure device reliability. As a result, analog circuit and mixed signal system designers are faced with many challenges in finding new ways to build analog circuits that can operate at lower supply voltages while maintaining performance. Bandgap references are subject to these headroom problems especially when the required supply voltage approaches the Bandgap voltage of silicon i.e. 1.25V. This paper presents a review of constraints, limitation factors and challenges to design a sub 1 V CMOS Bandgap Reference (BGR) circuits in todays and future submicron technology.*

II. INTRODUCTION

The band-gap reference has been a popular analog circuit for many years. In 1971, Robert Widlar introduced the LM113, the first band-gap reference. It used conventional junction-isolated bipolar-IC technology to make a stable low-voltage (1.220V) reference. This type of reference became popular as a stable voltage reference for low-voltage circuits. Bandgaps are also used in digital ICs such as ECL, to provide a local bias that is not adversely affected by ambient noises or transients. An important part in the design of analog integrated circuits is to create reference voltages and currents with well defined values. To accomplish this on-chip, so called Bandgap reference circuits are commonly used. These circuits allow the design of temperature independent reference voltages. A typical application for this reference voltage is in analog to digital conversion, where the input voltage is compared to several reference levels in order to determine the corresponding digital value. The objective of this review lies on theoretical understanding of performance limitations and to design a BGR circuit. In this review, a comprehensive study of Bandgap circuits and BGR principles is done.

III. BASIC BANDGAP REFERENCE CIRCUITS

The two most popular voltage references are Zener-based Voltage reference and Band gap Voltage reference. The Zener-Based Voltage Reference is simplest and the conventional form of a voltage reference. Fig. 1.1 [1] shows a buried Zener voltage reference and the diode is biased by a current source.

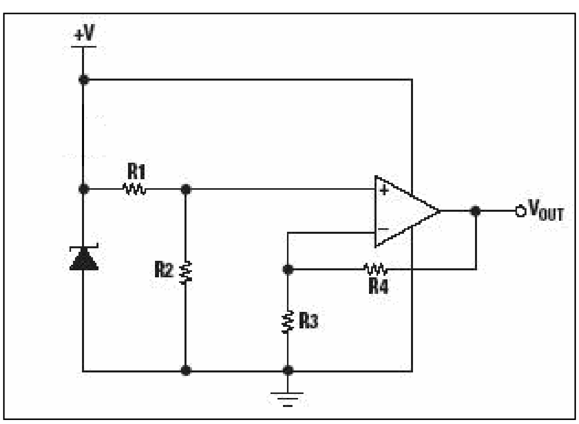

Fig.1.1 – Buried Zener reference circuit

$$Vout = \frac{R_2}{R_1 + R_2}\left(1 + \frac{R_4}{R_3}\right) \times V \quad \text{...............(1)}$$

The Zener diode called buried diodes as they are fabricated beneath the surface of the chip. The ones fabricated on the surface are noisier as they can get contaminated easily. The buried diode references are more expensive than the Bandgap references but are more accurate. Buried Zener diodes can be made with a range of voltages and have good low noise performance (better than Bandgap references), but the ones that, in combination with their temperature compensating diodes, have a breakdown voltage just below 7 V, have the best temperature performance. But their biggest limitation is the minimum supply voltage required. They need a supply voltage of at least 6 V. In today's technology the supply voltages are always shrinking and 6 V is just not the norm. Thus these types of references are no longer used. Whereas Bandgap Voltage Reference circuit is one where two quantities with opposite temperature coefficients are added with a proper weighing factor to result in a temperature coefficient of approximately zero. This can be explained as two quantities B1 and B2 having opposite temperature coefficients and choosing the coefficients c1 and c2 in such a way that the reference voltage Vout = c1V1+c2V2 has a zero temperature coefficient.

$$c_1 \frac{\partial B_1}{\partial T} + c_2 \frac{\partial B_2}{\partial T} = 0 \quad \text{............................(2)}$$

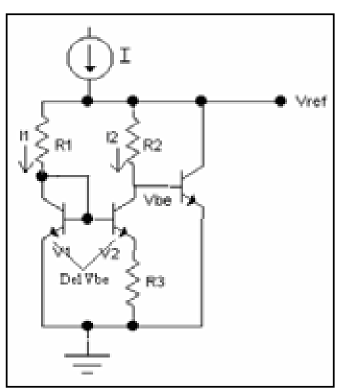

Fig.1.2 Basic Bandgap Circuit

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Fig. 2.2 shows a Bandgap circuit in its very basic form. Here the Vbe, which has a negative temperature coefficient is complementary to absolute temperature and the delta Vbe is proportional to absolute temperature and a weighted addition of both results in the Vref with a near zero temperature coefficient.

II. DESIGN CHALLENGES OF SUB 1 V CMOS BANDGAP REFERENCES(BGR)

Reference voltage generators are required to be stabilized over process, voltage and temperature variations, and also to be implemented without modification of fabrication process. The conventional output voltage of BGR circuit is 1.25 V, which is nearly the same voltage as the Bandgap of silicon. This fixed output voltage of 1.25 V limits the minimum supply voltage (VDD) operation. In addition, since the main popular trends in the design of BGR circuits rely on the usage of an operational amplifier (OpAmp) in the PTAT current generation loop, the offset of the Opamp greatly affects the accuracy of the BGR circuit. Moreover, the currents mirrors mismatch, the resistors mismatch, the transistors mismatch, the emitter-base voltage (VEB) spread, and the package shift are among the main dominant sources of errors affecting the performance of BGR. Some of the desired characteristics of a voltage reference are : Ability to be implemented in silicon, accuracy and stability over supply voltage, proper startup value and accurate over a wide range of temperature.

The relative stability of a BGR circuit is determined by the temperature coefficient of the reference over the operating temperature range, the power supply noise rejection (PSR) over the operating voltage range, the load regulation over the range of output load impedances, and the peak-to-peak output noise generated by the intrinsic noise sources of the circuit.

III. DESIGN OF SUB 1 V CMOS BANDGAP REFERENCES

An ultra low power (200 nA current consumption) reverse Bandgap voltage reference is proposed by Vadim Ivanov [1]. In this new reference circuit is able to operate down to supply voltages as low as 0.75V. The BGR reference is a part of microprocessor system on chip implemented in a digital 130 nm CMOS process and has a total area of 0.07 mm^2. The BGR accuracy is 2.5% (5 sigma) over a temperature range of 20 to 85^{0}C without trimming is reported. With trimming 0.5% accuracy is achieved. The circuit consumes 170 nW of power and the reverse Bandgap operation principle for reference generation enables the best accuracy in the sub-volt class of voltage references. In this paper author used switched-capacitor techniques for reference generation is not only solving limitations imposed by the digital CMOS process, but also allows to decrease the minimum operating voltage by 150 mV. This technique well aligns to the introduced S/H buffer approach which enables the design of a voltage reference with nano-power consumption while preserving low noise and high accuracy. A simplified circuit of the reference core is shown in Fig. 3.1. It contains the bias current generator (Q_0, R_0, M_0 - M_5), which creates $I_0 = V_{BE} / R_0$. The voltage across resistor is equal to of the bipolar transistor Q_0 and has a negative temperature coefficient. Due to the very high TC of polysilicon resistors in the used process the biasing current has positive TC.

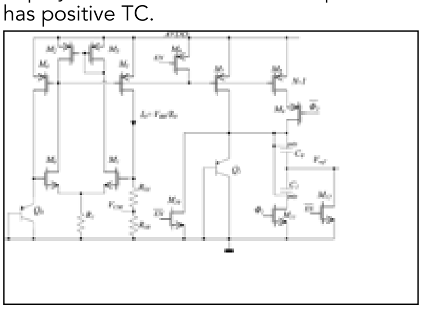

Fig.3.1. Reference core [1]

In the reference [2] authors Guang Ge et al. proposed a CMOS Bandgap reference with an inaccuracy of 0.15% (3 sigma) from 40^{0}C to 125^{0}C. In contrast to prior art, it requires only a single trim to achieve this level of precision. In this paper authors reported detailed analysis of the various error sources and techniques to reduce them. The prototype Bandgap reference draws 55μA from a 1.8 V supply, and occupies 0.12 mm^2 in a 0.16 μm CMOS process. A high precision CMOS Bandgap reference has been presented. Overall paper explained three key aspects: room temperature trim to remove the PTAT errors, chopping to reduce the offset of the opamp in the Bandgap core, and curvature correction to minimize the temperature nonlinearity of the base-emitter voltage. Author reported the chopping technique which is used to reduce the opamp offset, as shown in Fig. 3.2. Compared to auto-zeroing, chopping results in superior noise performance, while simultaneously ensures that the opamp's output is continuously available. A folded cascode opamp with a DC gain of 80 dB is used in this design.[2]

Author David C. et al. [3] present a low-power Bandgap reference (BGR), functional from sub-1V to 5 V supply voltage with either a low dropout (LDO) regulator or source follower (SF) output stage, denoted as the LDO or SF mode, in a 0.5um standard digital CMOS process with 0.6V and 0.7V at 27^{0}C. Both modes operate at sub-1V under zero load with a power consumption of around 26μW.

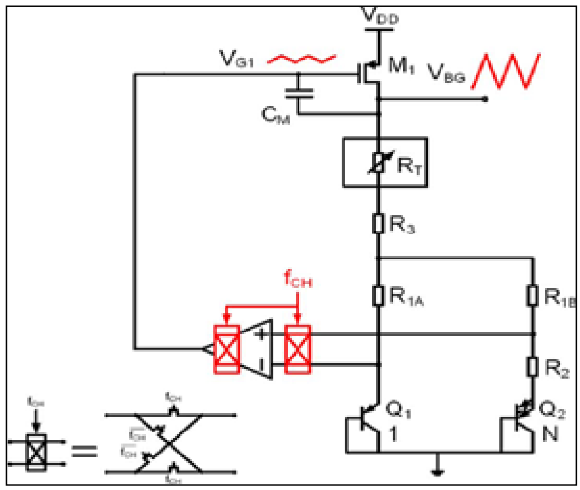

Fig.3.2. Bandgap reference with a chopped opamp[2]

At 1 V (1.1 V) supply, the LDO (SF) mode provides an output current up to 1.1mA (0.35 mA), a load regulation of 8.5 mV/mA (33mV/mA), a line regulation of 4.2 mV/V (50 V/V), and a temperature compensated reference voltage of 0.228 V (0.235 V) with a temperature coefficient around 34 ppm/ ^{0}C from 20^0 C to 120^{0}C. At 1.5 V supply, the LDO (SF) mode can further drive up to 9.6 mA (3.2 mA) before the reference voltage falls to 90% of its nominal value. Author claim that such low-supply-voltage and high-current- driving BGR in standard digital CMOS processes is highly useful in portable and switching applications.

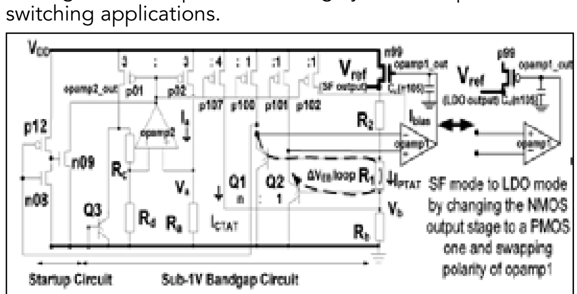

Fig.3.3. Proposed SF/LDO mode BGR [3].

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In the reference [4] the proposed design is implemented using 180nm technology using Cadence tool. The author Rohini Hongal et al. claimed that the reference voltage variation with respect to temperature in terms of 'uV' and consuming 54μW power. The architecture also incorporates the facility to switch on and off the entire circuit with 6μS settling time. Mis-matching of PMOS current mirrors

and resistor variation with respect to temperature could limit the accuracy of voltage reference. The given architecture can be used to generate sub Bandgap voltage references as it operates in the current mode. Therefore circuit is well suited for low voltage and low power applications. Still accurate references can be generated by incorporating resistor trimming network and MOS selection network to reduce the variation w.r.t temperature and supply voltage respectively.

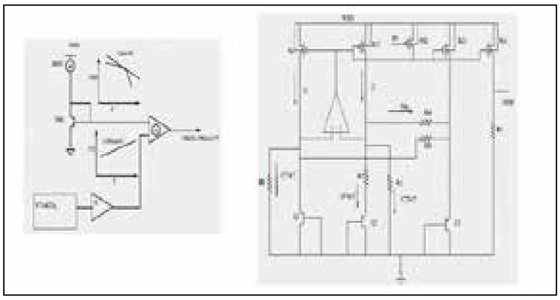

Fig.3.4 Basic principle of Bandgap Reference & Architecture of Curvature Corrected BGR [4]

A low-voltage, low power all MOS transistors Bandgap reference circuit in the standard 0.13μm CMOS process is reported by H. D. Roh, et al. [5]. Author is used MOSFETs which work in weak inversion region instead of BJTs and diodes. As a result, the low supply voltage 0.6V Bandgap reference circuit with all MOS transistors appears in this paper. What's more, in this paper the chopper stabilization technique is proposed to minimize the errors brought by the OTAs of both Bandgap reference circuit and unity buffer, thereby a good performance Bandgap reference circuit arises. Author reported the chopper stabilization technique greatly reduce the errors comparing to the bangap reference circuit without chopper switches. The BGR circuit as shown in Fig. 3.5 is reported.

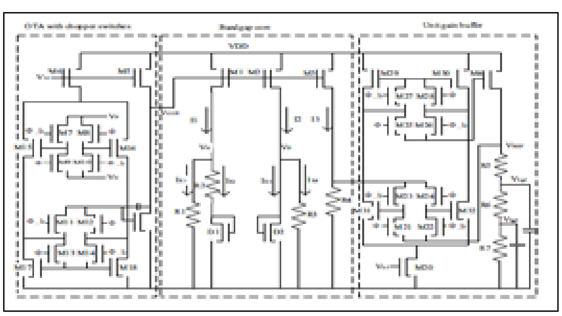

Fig. 3.5. Schematic of BGR using chopper stabilization technique [5]

Savvas Koudounas et al. [6] propose a new CMOS Bandgap Reference Generator topology that allows a straightforward implementation of an exact curvature compensation method by using only poly-silicon resistors. This is achieved by using a second Opamp that generates a CTAT current, which is subsequently used to enhance the curvature compensation method. Author also claimed that proposed technique is superior than previously proposed architectures is achieved with respect to temperature sensitivity of the reference voltage. In nominal simulations, that was less than 0.1ppm over a temperature range of -40^{0}C to 125^{0}C for a CMOS 0.35μm technology. In practice, the proposed BGR as shown in Fig. 3.6 is sensitive to device mismatch and thus resistor trimming is necessary if high performance is required.

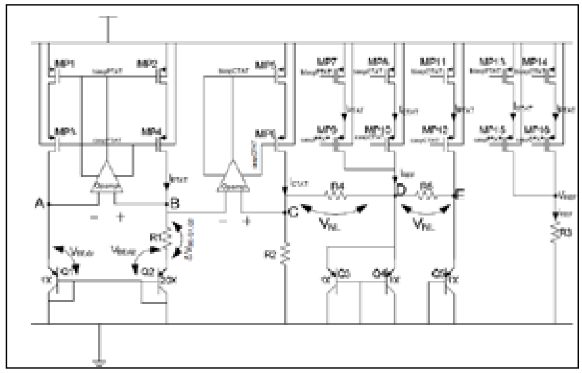

Fig 3.6. BGR with High-Order Temperature Compensation [6]

An area-efficient CMOS Bandgap reference (BGR) with switched-current and current-memory techniques is reported in the paper [7]. Author uses only one parasitic bipolar transistor to generate a reference voltage so that significant area reduction can be achieved. In addition, bipolar transistor device mismatch can be eliminated. The circuit as shown in Fig. 3.7 is produces an output of about 650 mV, and simulated results show that the temperature coefficient of the output is less than 10.4 ppm/^{0}C in the temperature range from 0^{0}C to 100 ^{0}C. The average current consumption is about 49.5μA in the above temperature range. Furthermore, the output can be set to almost any value. The circuit was designed and simulated in 0.25-μm CMOS technology. The layout occupies less than 0.0011 mm2 (100μm× 110μm) area is reported.

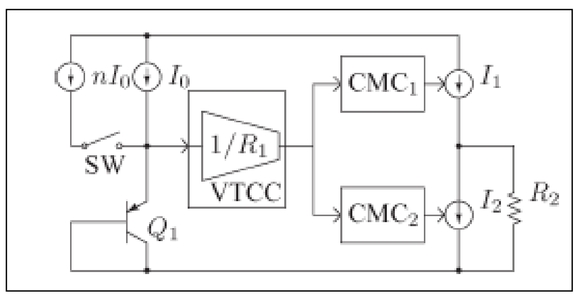

Fig.3.7. Conceptual diagram of BGR. [7]

The novel BGRs have been designed successfully by Yat-Hei Lam et al. in reference [8] using a self biased SM CVM. The systematic offset and power supply sensitivity were minimized due to the symmetrical circuit structure. Their performances were estimated by small-signal analysis and were experimentally characterized and compared with a conventional 4T BGR design, showing that the proposed designs had improved supply rejection, current efficiency, and reduced output impedance (for BGRs with buffered output). The design methodology was also extended to achieve a sub-1-V BGR that could be employed in low-voltage applications. An excellent line regulation is presented. By replacing the operational amplifier with a CVM in the feedback loop, current consumption is much reduced. The technique is extended to design a sub-1-V BGR with a TC-cancellation output buffer. All circuits as shown in Fig. 3.8 are designed using a 0.35μm CMOS process.

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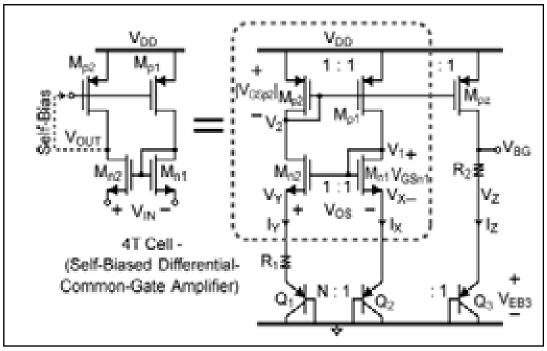

Fig.3.8. BGR with 4T cell (4T BGR) [8]

IV. SUMMARY

Bandgap voltage references (BGR) are circuits that provide a temperature and supply insensitive output voltage. Voltage references are among the most important building blocks in analog circuits and are used in dynamic random access memory (DRAM), flash memories, power supply generation, DC bias voltage, and current sources, analog-to digital converters (ADCs), and digital-to-analog converters (DACs). In addition, the performances and precision of coders and/or decoders, as well as the conversion accuracy of signal processing blocks in data converters systems are strongly dependent on the accuracy of the reference voltage. Traditionally, the output reference voltage has always been approximately equal to the intrinsic Bandgap voltage of the semiconductor material used, the silicon for instance. In Bandgap reference, an output voltage with low sensitivity is obtained as the sum of a voltage that is proportional to absolute temperature (PTAT) and a voltage with negative temperature coefficient, which is complementary to absolute temperature (CTAT).

A detailed summary on the state-of-the-art BGR circuit is given in Table 1. We have provided an in depth survey of the existing BGR circuit design techniques, which give insights a designer can relay upon when building CMOS voltage reference. In this report effort is made to understand various topologies of the existing Bandgap reference circuits and identify the limitations which make these circuits difficult to use with current processes, mainly with sub-1V technologies.

Table 1 Performance summary Bandgap voltage reference circuits design techniques

Reference	Technology	Ref voltage	Power Supply	Line Regulation	Load regulation	PSRR	Area	TC(ppm/^{0}C)	Power Consumption	Methodology
[1] July-2012	130nm CMOS	256mV	0.75V	-	-	50ppm/V	0.07 mm^2	40ppm/°C -20°Cto85°C	0.17uW	Reverse Band Gap, accuracy achieved by trimming
[2] Nov-2011	0.16um CMOS	1.0875 V	1.8V	-	-	74dB@DC	0.12m m^2	5-12ppm/°C -40°Cto125°C	55uA@1.8 V	Single Trim BGR with 3σ inaccuracy
[3] July-2011	0.5um CMOS	0.228V	0.93V to 5V	±4.2mV/V	±14.6@VDD=0.96 V ±1.2@VDD=1.5V	-58dB @100Hz -12dB @ 1MHz	0.0464 mm^2	34ppm/°C -20°Cto120°C	26uW	Low drop out regulator
	0.5um CMOS	0.235V	0.93V to 5V	±50uV/V	±33@VDD =1.1V ±3.6@VDD=1.5V	-58dB @100Hz -18dB @ 1MHz	0.0445 mm^2	34ppm/°C -20°C to120 °C	26uW	Source follower mode
[4]-2010	0.18um CMOS	1.1V	1.8V	-	-	-	0.048 mm^2	0.55ppm/°C -40°Cto125°C	54uW	Curvature Corrected BGR
[5]-2010	0.13um CMOS	300mV	0.6V	-	-	-	-	-	8uW-	Chopper Stabilization technique
[6]-2010	AMS,CMOS 0.35um	600mV	2.5V	-	-	-	0.1019 mm^2	0.08ppm/ °C -40 °C to 125 °C	95.875uW	Improved high order temperature compensation
[7] Oct-2010	0.25um CMOS	0.65V	3V	-	-	-51dB @1KHz	0.011 mm^2	10.4ppm/^{0}C 0 °C to 100 °C	138.6uW	Switched Current Technique
[8] Jun-2010	0.35um CMOS	1.2V	1.75V to3.5V	28mV/V	-	-26.2dB	0.0206 mm^2	12.85 ppm/ °C 5 °C to 95°C	162uW	4TBGR
				1.8mV/V	-	-51dB	0.02 mm^2	12.67 ppm/ °C 5 °C to 95°C		SMI BGR
				1mV/V	4mV/mA	-53.30 to -57.85dB	0.0432 mm^2	12.1-38.3 ppm/ °C 5 °C to 95°C		SMB BGR
		0.635V	0.9V to 3.5V	3.5mV/V	7 mV/mA	-47.6mV	0.059 mm^2	24.6-20 ppm/ °C 5 °C to 95°C		LV-SMB BGR

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