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An Efficient High Power Factor AC-DC Boost converter by Current Sensing Technique for Vehicle and Residential Charging Application

KEYWORDS AC–DC converter, boost converter, DC-DC converter, Bridgeless power factor correction (PFC), current sensing, plug in charger.

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ABSTRACT *This paper proposed a semi-bridgeless boost power factor corrected converter (PFC) with phase shifting. This converter is operated with simplified current-sensing method for the semi-bridgeless boost PFC converter. The proposed converter has the advantageous features such as high efficiency at light loads and low ac input lines, minimize the charger size, charging time, and less amount and cost of electricity drawn .This paper presented a simulation results of a boost converter, converting the 230V ac input voltage to 400 V dc at 1 kW to 3kW Load.*

I.INTRODUCTION

A storage system that can be recharged by connecting a plug to an external electric power source. The charging AC outlet predictably needs an plug in AC/DC charger with a power factor correction [1].[2]. For the PFC application a multiple of circuit topologies and control methods have been developed. The single-phase active PFC techniques can be classified into two approaches: they are single-stage approach and the two-stage approach. The single-stage approach is right for low power level applications. It can only applicable for lead acid batteries charging because of frequency ripple problem. Therefore, the two-stage approach is the suitable for high storage battery chargers used for high power applications, where the power rating is relatively high, and lithium-ion batteries[3] are used as the main energy storage system. In the two-stage architecture, the first stage is PFC rectification where it rectifies the input ac voltage and transfers it to a dc-link. At the same time, the PFC is also achieved [4]. A phase shifted semi bridgeless PFC topology operated under continuous conduction mode as the two stage charger specifically with the ac–dc PFC converter and dc-dc converter for battery charging with various duty cycles.

1 .Interleaved PFC boost topology

This boost topology uses two boost converters in parallel operating 180◦ out of phase [5]–[7]., by switching 180◦ out of phase, it doubles the effective switching frequency and introduces a smaller input current ripple; thus, the input electromagnetic interference (EMI) filter can be smaller than a single PFC boost topology [8]–[10]. The drawback of this topology is the very high loss and the resultant heat management issue for the input diode bridge rectifiers. Fig 1 shows simulation of interleaved topology.

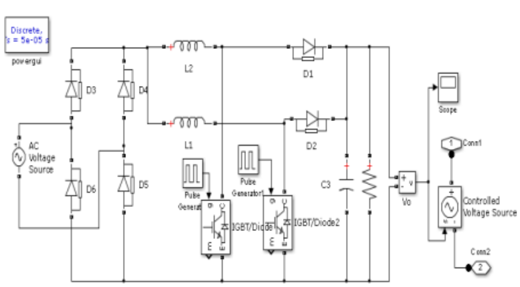

Fig .1.Simulation of interleaved topology

2. Bridgeless PFC boost topology

This bridgeless boost topology avoids the need for the rectifier input bridge but maintains the classic boost topology [11]–[21]. The bridgeless boost converter, which is also called as the dual- boost PFC converter, which overcomes the problem of heat management in the input rectifier diode bridge, but it introduces increased EMI [22]–[24].

The common-mode (CM) noise generated by bridgeless PFC is much higher than the conventional boost PFC topology [24]. Drawback of this topology is the floating input line with respect to the PFC stage ground, which makes it impossible to sense the input voltage without a low-frequency transformer or an optical coupler.Fig2. represents the simulation of bridgeless PFC topology.

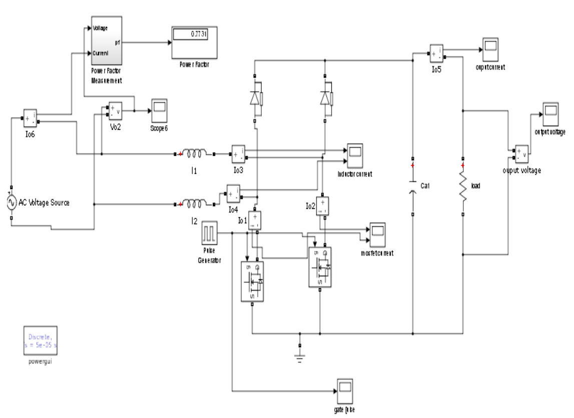

Fig.2.simulation of bridgeless PFC topology

3. Dual-boost PFC topology

The advantage of dual-boost PFC topology is [25] minimizes the gate loss, reduces the losses at light loads, the conduction loss can be minimized. The light-load efficiency improved by external device, which leads cost expense and improve controller complexity.

4. Semi-bridgeless PFC boost topology

Semi-bridgeless PFC boost topology is the conventional bridgeless topology with two extra slow diodes, that is , Da and Db, that connect the input to the PFC ground. The slow diodes were added to address EMI- related issues [22], [23].

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The current does not return through these diodes; therefore, their related conduction victims are small. The semi-bridgeless configuration also resolves the suspended input line problem with respect to the PFC stage ground. Fig 3.represents the simulation of semibridgeless PFC topology.

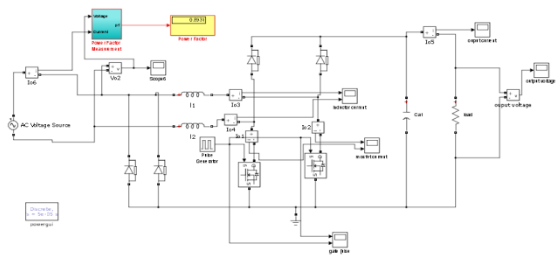

Fig3.simulation of semibridgeless PFC topology.

5. Current sensing techniques

Three exclusive current-sensing circuits (Methods 1–3) for the bridgeless PFC boost topology are shown in Fig. 4 to sense the current in the MOSFET and diode paths independently, as the current path does not share the similar ground throughout each half-line cycle [13], [26].

Method 1 Fig4 (i) is the passive current-sensing scheme reported in [13], which requires three current-sensing transformers—one in series with each switch and a third in the positive dc rail to sense the collective current of the two diodes, and an supplementary signal transistor with its related difficult control circuitry.1

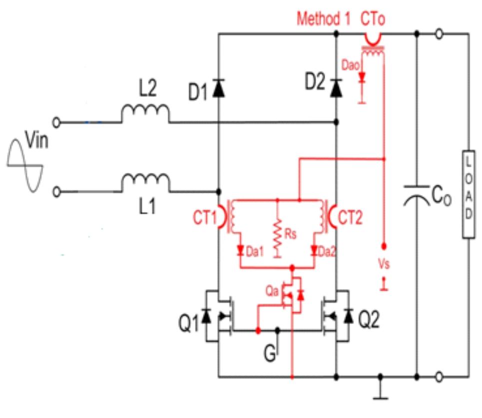

Fig 4(i) current-sensing method.1 implemented with bridgeless PFC topology.

Method 2 Fig4(ii) uses a simple, but costly, Hall Effect sensor to straightly sense the input current.

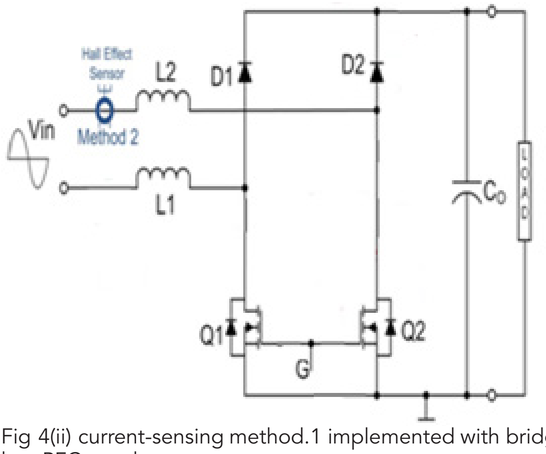

Fig 4(ii) current-sensing method.1 implemented with bridgeless PFC topology.

Method 3 Fig4(iii) uses a differential-mode amplifier ,which is connected in series with the input. This method is moderately less cost.

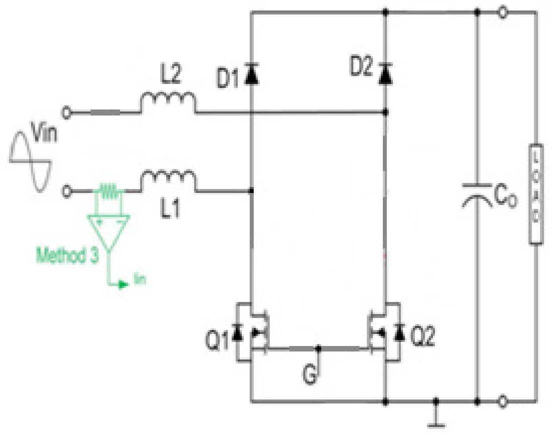

Fig 4(iii) current-sensing method.3 implemented with bridgeless PFC topology.

Where the current-sensing voltage is small to reduce the power loss, the power factor can be ruined by the sensing noise.

II-PROPOSED SYSTEM

The below diagram Fig[5] represents the general charging system for vehicle battery charging. Vehicle storage charging is one f the application of this converter[29]. The Fig[6] represents the block diagram of Phase Shifted boost power factor corrected converter .

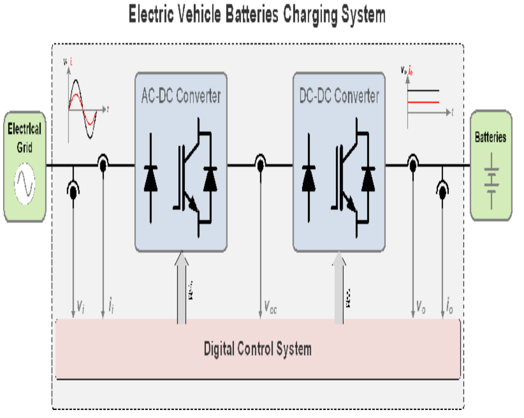

Fig.5 charging system

PSSB BOOST CONVERTER

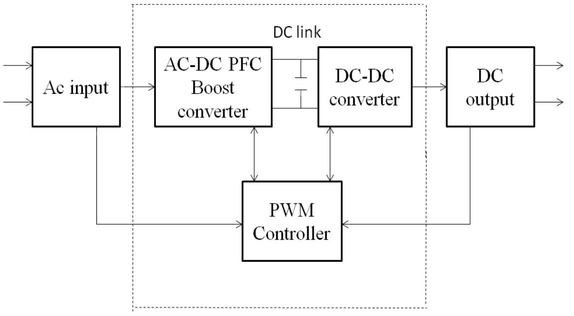

Fig.6 PSSB-block diagram

The proposed PSSB topology shown in Fig.6 is used the current sensing method [27]. This method is used to find the inductor current by sensing the MOSFET current [28].

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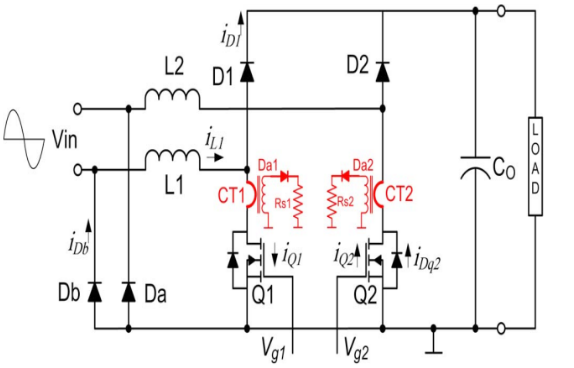

Fig. 7. Proposed PSSB PFC boost topology with a simple current-sensing circuit.

This topology consists the decoupled MOSFET gates, it uses two slow diodes (Da and Db), like to that of the semi-bridgeless PFC boost, to link the ground of the PFC to the input line. The gating signals for the MOSFETs are 180° out of phase, as shown in Fig. 8.

The proposed topology consists the advantages of both the bridge- less and semi-bridgeless boost PFC topologies.

Its features are reduced EMI, high efficiency at light loads, and low lines, which is critical to minimize the charger size, cost, charging time, and amount and cost of electricity drawn.

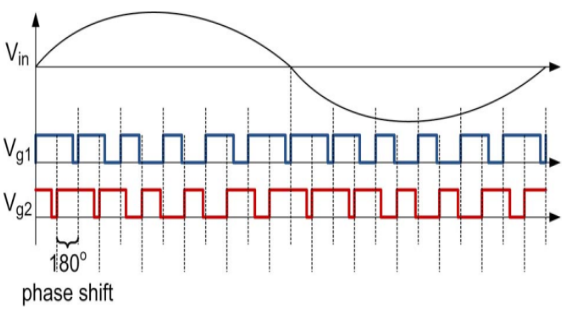

Fig. 8. Gating scheme for the PSSB PFC topology.

The following section includes operation of the proposed converter and converter simulation and its output.

III-OPERATINON OF CONVERTER

The proposed topology uses two slow diodes (Da and Db) to connect the ground of the PFC to the input line. The current does not return through these diodes, so their related conduction losses are low. The gating signals for MOSFETs are 180° out of phase. To evaluate the circuit operation, the input line cycle has been divided into the positive and negative half-cycles. The full circuit operation depends on the duty cycle.

POSITIVE HALF CYCLE OPERATION

During the positive half-cycle, when the input voltage is positive, Q1 turns on and current flows through L1 and Q1 and continues through Q2 and then L2, returning to the line while storing energy in L1 and L2. When Q1 turns off, energy stored in L1 and L2 is released as current flows through D1, through the load and returns through the body diode of Q2/ partially through Db back to the input.

NEGATIVE HALF CYCLE OPERATION

During the negative half-cycle, when the AC input voltage is negative, Q2 turns on and current flows through L2 and Q2 and continues through Q1 and then L1, returning to the line while storing energy in L2 and L1. When Q2 turns off, energy stored in L2 and L1 is released as current flows through D2, through the load and returns split between the body diode of Q1 and Da back to the input. Detailed Positive Half Cycle Operation and Analysis for D > 0.5 and D < 0.5 is analyzed in [29].

IV-SIMULATION OF PSSB BOOST SYSTEM

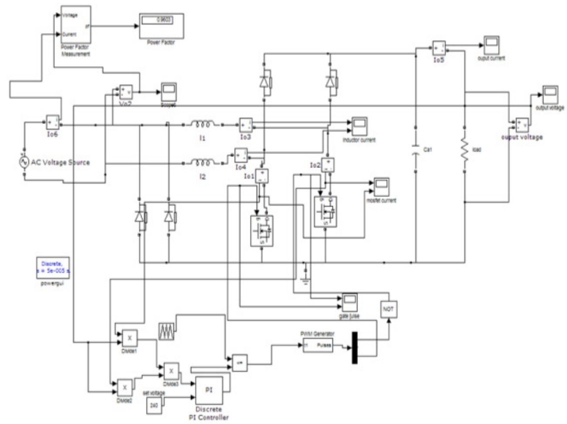

Fig.9. Simulation of PSSB PFC boost topology

Simulation of phase shifted semi bridgeless boost pfc converter simulate for 1KW load in MATLAB. Fig[10] shows the gating signal for 180 degree phase shift.

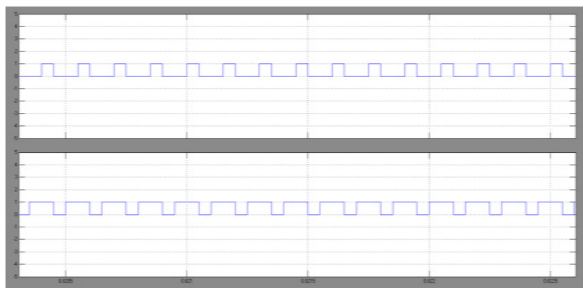

Fig10.gate signal waveform

Simulation results shown fig 11 input voltage ,fig 12 inductor current,fig 13 mosfet current,fig14 output voltage.

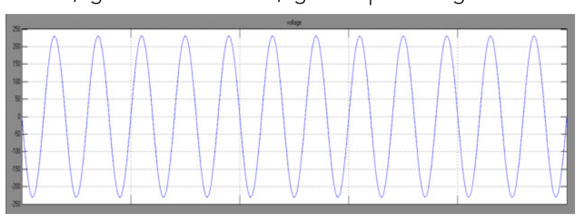

Fig11. Input voltage

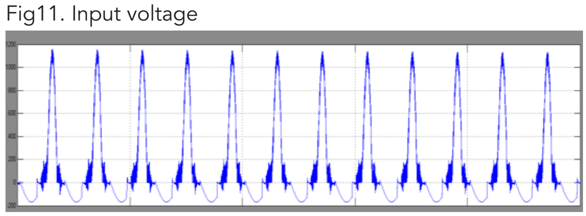

Fig.12 Inductor current

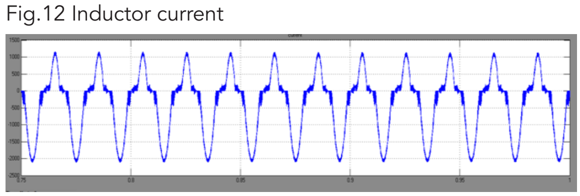

Fig.13 Mosfet current

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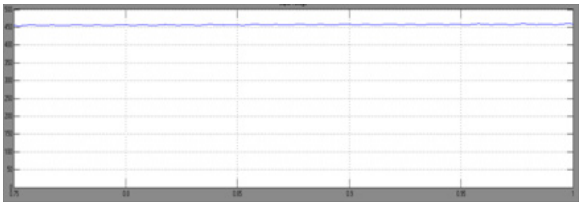

Fig.14 Output voltage

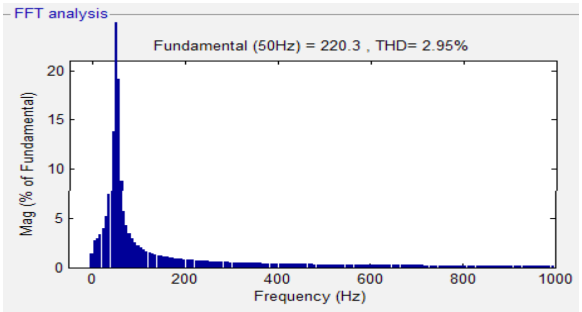

Fig.15 THD WAVE FORM

V-CONCLUSION

A better-performance Phase Shifted Semi Bridgeless boost converter topology has been proposed with simplified current sensing method. The converter advantageous features are high efficiency at light-load and low-line conditions, small in charger size, less cost, less charging time, and less cost of electricity. The input supply of the converter is 230V. While using this proposed converter system current THD is less than 5% for 1KW to 3KW load. The power factor is greater than 0.9 from 50% load to full load.

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