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Effect of Annealing and Deposition Temperature on Structural Properties of Cdte Thin Films Prepared by Thermal Evaporation Method

KEYWORDS: CdTe, thin film, annealing temperature, Thermal evaporation, silicon

Mustafa M. A. Hussein.	Manal M. Abdullah	Ghuson H. Mohammed
Department of Physics, College of Science, University of Baghdad	Department of Physics, College of Science, University of Baghdad	Department of Physics, College of Science, University of Baghdad

ABSTRACT *CdTe thin films are deposited at room temperature on both glass and p-type silicon wafer with different thicknesses by Thermal Evaporation technique. The thickness of films is set to be 100, 300, 500, and 700nm measured by Crystal Quartz method. The effect of the substrate temperatures (Ts= 100, 200, and 300°C) on the structural properties of films is studied by Ellipsometer. The results show decreasing in the adhesion force between thin film and substrate when Ts is increased especially for thicker films. For as deposited films, samples are annealed in air for one hour at annealing temperatures (Ta=100, 150, 200, 300, 400, and 500°C). It is found that for low thickness of CdTe layer in the range between (100 and 500nm), the best results are found at (Ta=300C) as shown by XRD patterns and surface profilometer images. Also we get best results for samples with thickness of 700nm and temperature annealing at 100oC. While at (Ta=500°C), the crystalline form of the samples is damaged.*

Introduction

Semiconductor materials are of great interest for many practical applications such as solar cells, optical detectors, dosimeters for ionizing radiation, opto-electrical devices and lasers [1–3]. Cadmium telluride has gained considerable interest as one of the most promising II–VI semiconductors. It is important as an 'absorber' semiconductor because of its direct band gap (1.5 eV), large absorption coefficients and optical absorption edge. Hence, it is suitable for use in terrestrial solar cells [4, 5]. Also, there has been an increased interest in CdTe due to its application in opto-electronics and nuclear radiation detection, and its use as a substrate for the growth of HgCdTe, which is an important infrared detector material [6–8]. The effect of thermal annealing on metal III–V Schottky barrier diodes has been reported [9]. However, little attempt has been made to understand surface barriers, the effect of thermal annealing, and the role of different metals onCdTe [10–13]. Deviation of the surface of CdTe singlecrystals from stoichiometry, as a result of annealingat about 453 K, has been reported [14]. It iswell known that surface preparation stronglyaffects the properties of layers used to formmetal–semiconductor contacts and often controlsthe interface properties of these junctions [15–17]. Some authors reported that the crystallinity of the film is improved with the thickness of the thin film layer [18] and temperature [19]. Therefore, it would be of interest toinvestigate the effect of annealing athigher temperatures on the structural properties ofthe cadmium telluride devices.

In the present work, the structural characteristics of Si–CdTe junctions are investigated as a function of the substrate temperature and annealing temperature in air. The aim of the present work is to study the behavior of the junctions under the above-mentioned conditions.

2. Experimental

In this work CdTe powder is used to deposit thin films on both glass and p-type silicon wafer substrates by thermal evaporation method using NANO 38 deposition systemsupplied by Kurt J. Lesker Company.The rate of deposition is set to be 0.05nm/sec for 100nm, 0.09nm/sec for 300nm, 0.13nm/sec for 500nm, and 0.17nm/sec for 700nm film thickness respectively so that the total time of the deposition process takes about one hour. The thickness of layers is controlled by crystal quartz method.The glass slices are cleaned with alcohol using vibrational system. To prepare the silicon wafers for the deposition process, the Shiraki cleaning is done then they are itched by HF for one minute to remove the oxide layer from them.

Two different approaches are followed to investigate the temperature dependence of the samples preparation. (a), the substrate is heated during the deposition process when the system as whole is in vacuum.In addition to room temperature (RT), the temperatures 100, 200, and 300°C are also set to be as the Ts values.After the end of deposition, the thickness of layers is measured precisely by Ellipsometerusing the J. A. Woollam Co. manufacturers Spectroscopic Ellipsometer for non-destructive thin film material characterization. Then all samples are tested by XRD method using Ultima IV X-ray diffractometersupplied by Rigaku Co.

In (b), films are deposited under vacuum at RT and then annealed in air for one hour at annealing temperatures (Ta=100, 150, 200, 300, 400, and 500°C) using plate heater.After annealing process, samples are also tested by XRD method and also by Profilometer using Veeco Wyko NT8000Optical Profilersupplied by DYMEK Company LTD.

3. Results and discussion

The XRD patterns of CdTe thin films deposited on glass at different substrate temperatures (Ts =RT, 100, 200, and 300°C) are shown in figures 1 to 4, respectively. The thickness of these films is 100nm.

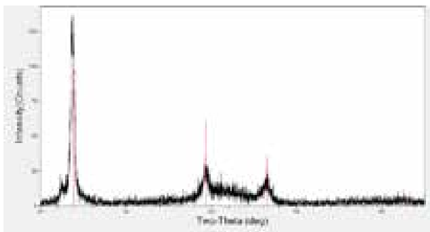

Fig.1: CdTe 100nm on glass, T_s=RT

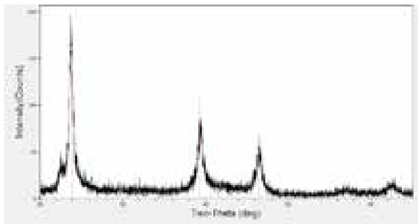

Fig.2: CdTe 100nm on glass, T_s=100°C

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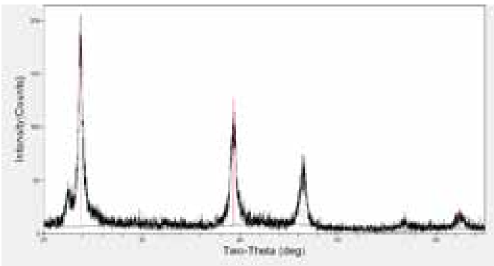

Fig.3: CdTe 100nm on glass, Ts=200°C

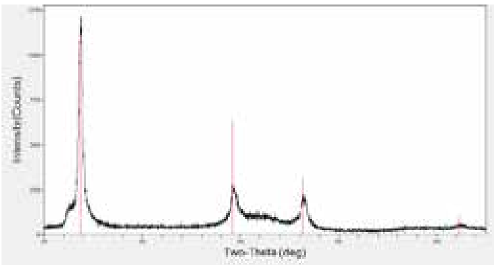

Fig.4: CdTe 100nm on glass, Ts=300°C

From these figures it is found that there are five diffraction peaks at different Bragg angles, 2θ=23.758, 39.311, 46.433, 56.820 and 62.351 degree corresponding to reflection surfaces (111), (220), (311), (400) and (331) respectively. And the films have crystallized with a strong peak at (111) directions, this means that this plane is suitable for crystal growth, which indicate that these films become polycrystalline.

The increase of the plane intensity for films could be attributed to the increase in crystalline grain size as the small crystals join each other due to films deposited at higher substrate temperature.

The inter planer spacing (d) of the CdTe thin films was determined from the Bragg relationships see eq. (1),

$2d \sin\theta = n\lambda$ ………… (1)

And comparison is made, as shown in table (1), between the inter planer distance calculated from the pattern of X-ray diffraction for all 2θ values and the standard which is deduced from ASTM cards.

Table (1): Comparison between calculated and standard values of inter planer distance, d, for XRD patterns of CdTe films for all 2θ values.

2θ(degree)	23.758	39.311	46.433	56.820	62.351
Calculated 'd' (A°)	3.741	2.289	1.953	1.618	1.487
Standard 'd' (A°)	3.742	2.290	1.954	1.619	1.488

Similar patterns are shown in figures 5 to 8, but this time films are deposited on silicon wafer. These patterns show increasing in crystallinity of films as Ts increases.

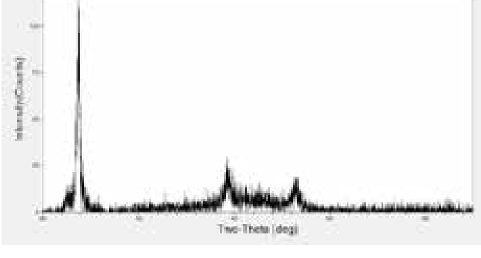

Fig.5: CdTe 100nm on silicon, Ts=RT

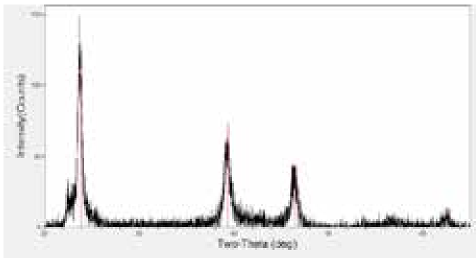

Fig.6: CdTe 100nm on silicon, Ts=100C

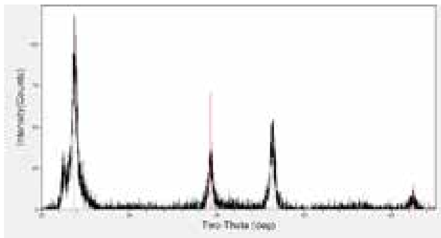

Fig.7: CdTe 100nm on silicon, Ts=200C

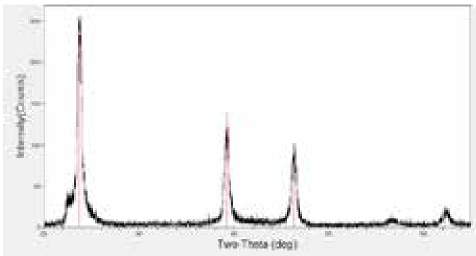

Fig.8: CdTe 100nm on silicon, Ts=300C

In order to study the adhesion force between the substrate and the thin film, the thickness of films is measured by Ellipsometer and it was 95nm for RT which is very close to the value predicted by Crystal Quartz method. While for other thicknesses and temperatures, the difference between these two values was apparently large especially for higher temperatures and thicker layers. For all thicknesses predicted by Crystal Quartz method, the real thicknesses measured by Ellipsometer were much less than the predicted values. This can be explained by decreasing in the adhesion force between thin film and substrate when Ts is increased, so that not all deposited particles are glued to the substrate. This decreasing in adhesion force is proportional to the thickness of the layer too. Table (2) shows a comparison between predicted and measured values of film thickness for the investigated temperatures.

Table (2):Comparison between predicted and measured values of film thickness for different T_s

Ts(°C) (Temperature of substrate)	Thickness of film predicted by Crystal Quartz (nm)	Thickness of film measured by Ellipsometer (nm)	Deviation percentage (%)
RT	100	95	5
RT	300	282	6
RT	500	465	7
RT	700	646	8
100	100	83	17
100	300	240	20
100	500	380	24
100	700	510	27.1
200	100	68	32
200	300	193	35.6
200	500	298	40.4
200	700	402	42.6
300	100	55	45
300	300	148	50.6
300	500	215	57
300	700	280	60

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So, in the next step (b), samples that prepared at RT are annealed in air at different temperatures, Ta, for one hour. Figures 9 to 14 show XRD patterns of samples after annealing.

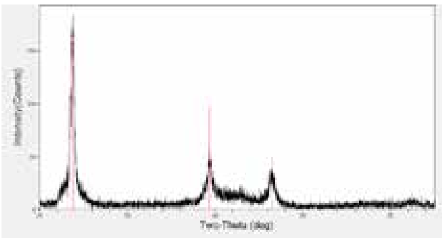

Fig.9: CdTe 100nm on Si, Ta=100°C

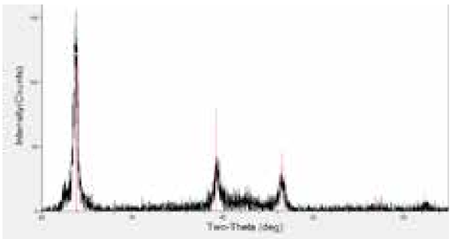

Fig.10: CdTe 100nm on Si, Ta=150°C

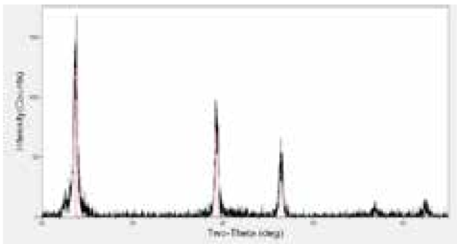

Fig.11: CdTe 100nm on Si, Ta=200°C

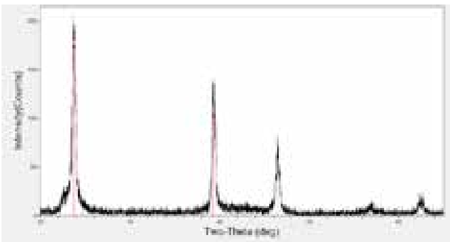

Fig.12: CdTe 100nm on Si, Ta=300°C

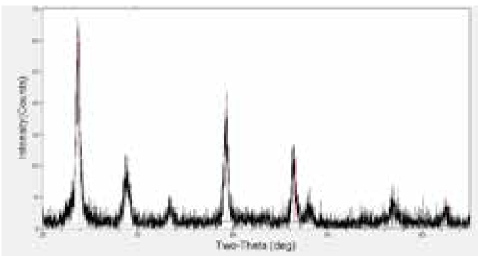

Fig.13: CdTe 100nm on Si, Ta=400°C

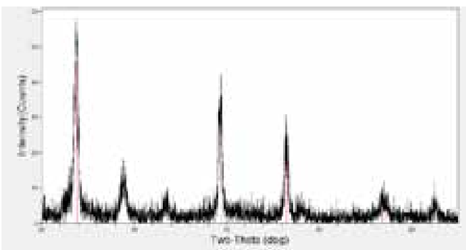

Fig.14: CdTe 100nm on Si, Ta=500°C

The best intensity could be seen in fig.12 at 300°C which is more than 200 counts, and the worst one is less than 60 counts at 500°C as seen in fig. 14. It can be concluded that the crystallinity of films is improved up to 300°C and then decreased. Also, at 500°C the sample is damaged because in some locations the layer is separated off the substrate.

In figs.15 to 21 the Surface Profilometer images of the samples at constant thickness of 100nm and different temperatures are shown.

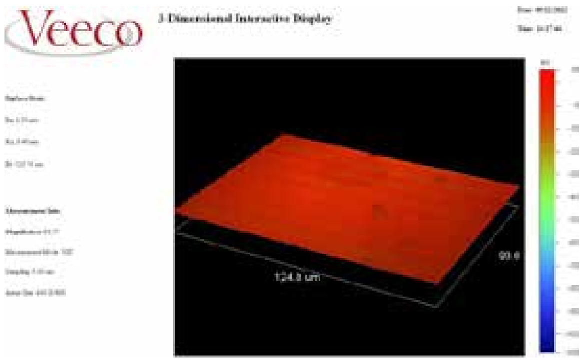

Fig.15: Surface Profilometer image at RT

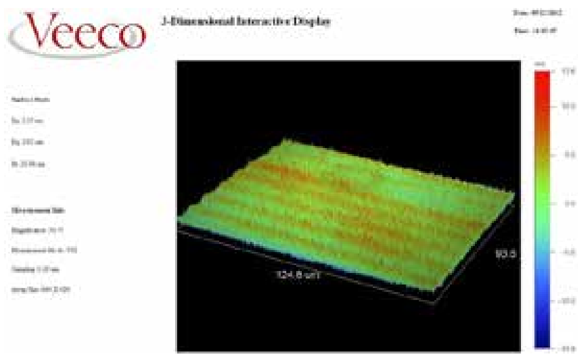

Fig.16: Surface Profilometer image at 100°C

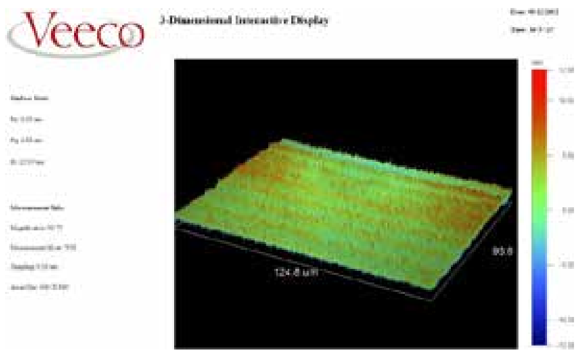

Fig.17: Surface Profilometer image at 150°C

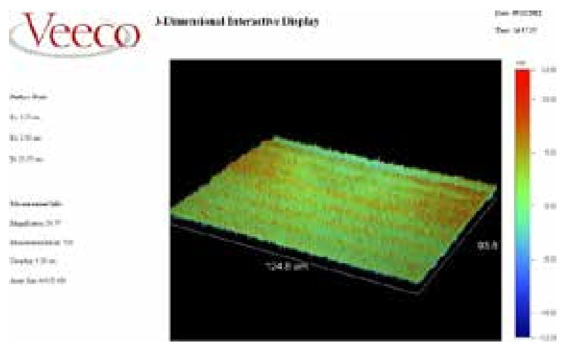

Fig.18: Surface Profilometer image at 200°C

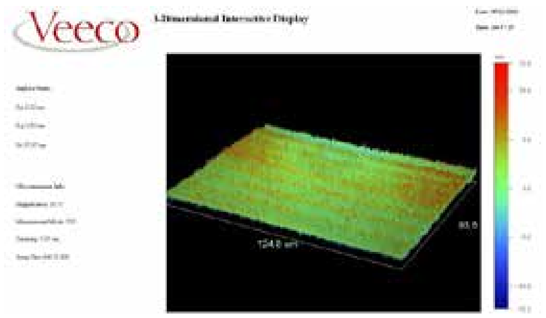

Fig.19: Surface Profilometer image at 300°C

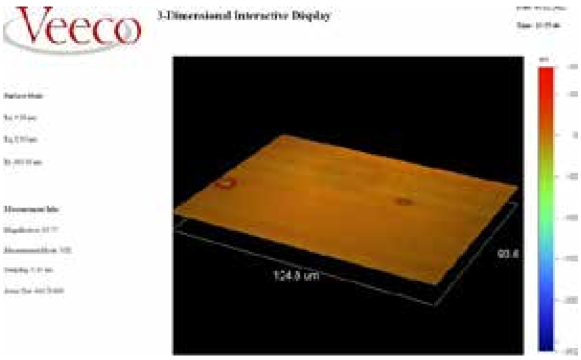

Fig.20: Surface Profilometer image at 400°C

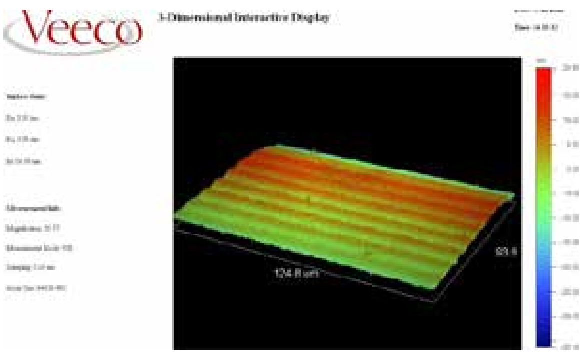

Fig.21: Surface Profilometer image at 500°C

From figure 21 and specifically from the red region, it is obvious that at 500°C there is a separation between the layer and substrate in some points. Also, the best values of surface parameters are seen at 300°C and figure 19.The most important surface parameters of Optical Profilometer are: Ra (average roughness), Rq (root mean square roughness), and Rt (extreme height value). Table (3) clarifies the relationship between Ta and roughness parameters.

Table (3): Parameters of roughness for thickness of film 100nm and different annealing temperatures.

Ta (°C)	RT	100	150	200	300	400	500
Ra (nm)	2.31	2.25	2.25	2.25	2.25	3.36	5.31
Rq (nm)	3.40	2.81	2.82	2.82	2.82	8.93	6.89
Rt (nm)	123.76	28.48	25.07	25.07	25.07	345.40	56.89

As mentioned before, annealing improves the crystallinity of these samples up to 300°C which is obvious from decreasing the values of roughness parameters. But for Ta values more than 300°C, it is clear that the values of roughness parameters increase and that means the crystallinity of samples is decreased.

Similar figures for other thicknesses give similar results except for 700nm which show best values of surface parameters at 100°C (Fig. 22). These results confirm the XRD results that we showed previously (figs.9 to 14).

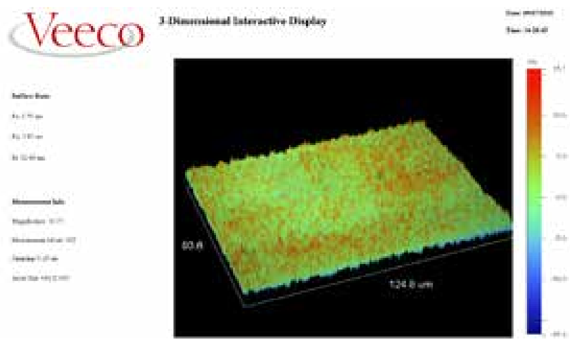

Fig.22: Surface Profilometer image at 100°C for 700nm CdTe film thickness.

4. Conclusion

The effect of increasing temperature of substrate while the system is in vacuum is the decrease of adhesion force between the substrate and the film. When temperature is fixed, the crystallinity of films is increased with the thickness.

By annealing samples in air, for thicknesses up to 500nm, the crystallinity of films is increased with temperature up to 300°Cand then decreased. For 700nm, the maximum of the crystallinity of films is at 100°C. At 500°C, all samples are damaged.

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