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A Comparative Study of 6T, 8T and 10T SRAM Cells based on Performance and Word Organization

KEYWORDS: SRAM, Static Noise Margin, Write Trip Point, SRAM word organization

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ABSTRACT *Now-a-days low power and high stability have been the main theme is designing SRAM, due to this we are moving towards the new technologies. As a result, we are facing new challenges in developing the new technologies. These technologies lead to the implementation of different types of SRAM's. From the last few decades, the scaling down of CMOS devices have been taking place to achieve better performance in terms of speed, power dissipation, size and reliability. Basically, the performance of the SRAM cell is measured based on Static Noise Margin and Write Trip Point. The stability of SRAM cell also depends on Static Noise Margin and Write Trip Point.*

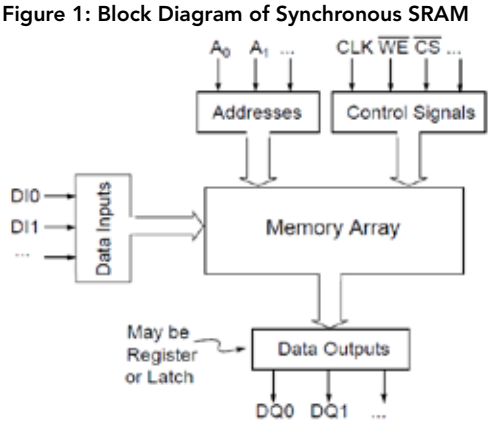
In this paper, the comparison of 6T, 8T and 10T SRAM cells has done on the basis of Static Noise Margin, Write Trip Point and SRAM word organization.

I. INTRODUCTION

As microprocessors and other electronics applications get faster and faster, the need for large quantities of data at very high speeds increases, while providing the data at such high speeds gets more difficult to accomplish. As microprocessor speeds increase from 25 MHz to 100 MHz, to 250 MHz and beyond, systems designers have become more creative in their use of cache memory, interleaving, burst mode and other high-speed methods for accessing memory.

Static random-access memory (SRAM) is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit. The term static differentiates it from Dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. There are many reasons to use an SRAM or a DRAM in a system design. Design parameters include density, speed, volatility, cost, and features. All of these factors should be considered before you select a RAM for your system design.

Figure 1: Block Diagram of Synchronous SRAM



The basic architecture of a static RAM includes one or more rectangular arrays of memory cells with support circuitry to decode addresses, and implement the required read and write operations. Additional support circuitry used to implement special features, such as burst operation, may also be present on the chip. Figure 1 shows a basic block diagram of a synchronous SRAM. As you read, you may wish to refer to the diagram to help you visualize how the SRAM works. SRAM memory arrays are arranged in rows and columns of memory cells called word-lines and bit-lines, respectively. In SRAMs, the word-lines are made from polysilicon while the bit-lines are metal. Each memory cell has a unique location or address defined by the intersection of a row and column.

Each address is linked to a particular data input/output pin. The number of arrays on a memory chip is determined by the total size of the memory, the speed at which the memory must operate, layout an d testing requirements and the number of data I/Os on the chip.

In designing a robust SRAM the challenge is to ensure a reasonable noise margin, which is normally measured by the Static Noise Margin (SNM) and the Write Trip Point (WTP) [1], [2]. According to [1], these two design factors they are linearly dependent on the supply voltage, reducing which to save power has a negative impact on the cell stability. As a result, it is extremely difficult to maintain the cell stability. Unfortunately, these two factors conflict with each other and hence improving one is likely to jeopardize the other. There are two commonly used ways to arrange the words in SRAM architecture: shared WL and bit-interleaving. Most of these designs can only be implemented in word-line (WL) sharing architecture which is not preferable as the conventional Error Correction Code (ECC) requires bit-interleaving to address multiple bit soft-error [3], [4], [5].

In this paper, we compared the performance and word organization in 6T, 8T and 10T SRAM cells and based on this comparison we conclude the better SRAM cell among them.

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II. CONVECTIONAL 6T SRAM CELL

Figure 2 shows the conventional 6T SRAM cell which has two back to back connection of inverters using N1, P1, N2, P2 to store the single bit either '0' or '1'. N3, N4 transistors are called as access transistors. WL is used to turn ON the access transistors. BL, /BL are bit lines.

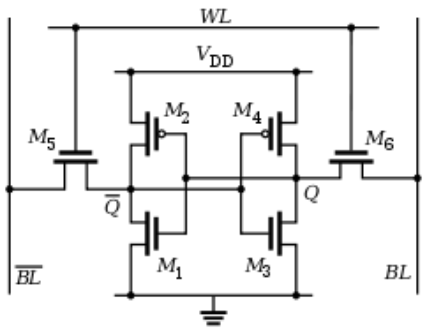
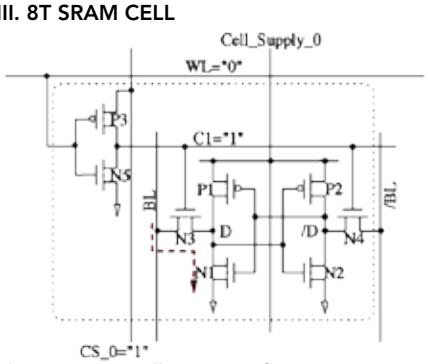


Figure 2: Conventional 6T SRAM Cell

An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows [6]

Standby: If the word line is not asserted, the access transistors M_5 and M_6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M_1 – M_4 will continue to reinforce each other as long as they are connected to the supply.

III. 8T SRAM CELL



The 8T SRAM cell consists of 8 transistors, N1-N5 and P1-P3, as shown Figure 3, four transistors N1, N2, P1, P2 form a cross-couple structure to store data. Four transistors P3 and N3- N5 are access to the internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes D and /D of the cell. N3 and N4 connect the cell internal nodes to the BLs while P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while gates of P3 and N5 are connected to WL. Unlike conventional design, the sources of P1 and P2 are connected to dynamic cell supply (cell_supply) line which is raised to the higher voltage during read operation to obtain a higher noise margin [4].

V. SNM AND WTP

The performance of the SRAM Cell is normally measured by two design metrics: SNM and WTP.

SNM measures how stable a cell is. It is defined as the worst case noise level available at the gates of the inverters that does not cause the cell to flip. Therefore, SNM is normally associated with the Read operation and it is desirable to have as high SNM as possible.

WTP on the other hand, measures how easy it is to write into a cell. When a cell is to be written, one of the BLs (e.g., /BL) remains at V_{DD} while the other (e.g., BL) is pulled to ground. WTP is defined as the highest BL potential that causes the cell data to flip successfully. It is also preferable to have as high WTP value as possible. A high WTP indicates that the cell can be written to easily and less voltage swing on the BL is required.

The 8T SRAM design improved both SNM (2x) and WTP (10%) with a marginal area overhead (14%) when compared to the conventional 6T design. In addition, only one cell is accessed during a read or write operation.

VI. WORD ORGANIZATION

There are two commonly used ways to arrange the words in SRAM architecture: shared WL (Figure 5(a)) and bit-interleaving (Figure 5(b)).

In the shared WL architecture, all the bits of the same words are located next to each other. For example, Figure 5(a) shows a row of k words, with each having n bit cells. During access, the WL is activated and all the bits on the row are turned on. A NAND gate can also be used to choose only one word out of k words on a row. This architecture is widely used because of its simplicity and compactness. However, as all the bits of a word are adjacent to each other, the probability of multi-bit soft errors is very high. This has a negative impact on the yield of the chip. As a result, bits of adjacent words must be interleaved to avoid the multi-bit errors in the accessed word so that conventional ECC can be implemented to detect the single error bit. For example, in Figure 5(a), if we read from word A_1 and the ionized radiation is focused on the first bit of the row (i.e., A_{11}), the adjacent cells are also affected. Thus, A_{12}, A_{13}.... A_{1p} may be erroneous too.

VII. CONCLUSION

In this paper, we have compared the Static Noise Margin (SNM), Write Trip Point (WTP) and Word Organization in 6T, 8T and 10T SRAM cells and also provide the working of these SRAM cells. The combination of SNM and WTP gives the performance of the SRAM cell, so the performance of the SRAM cell is dependent on the SNM and WTP. In 6T SRAM cell there are two drawbacks, 1.SNM and WTP are jeopardize to each other, so trying to improve one of them will have the negative impact on the other, this leads to the decrease in the performance of the SRAM cell and 2.It uses shared WL architecture in word organization. These two drawbacks are eliminated in the 8T and 10T SRAM cells as follows 1.The jeopardize nature of SNM and WTP are eliminated by providing separate read and write ports in the SRAM cells and 2.These SRAM cells uses the Bit-Interleaving architecture in word organization. 8T SRAM cell utilizes the less power and also the layout of the 8T SRAM cell is simple when compared to 10T SRAM cell as it utilizes the less number of transistors.

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