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Performance Evaluation of 6T Sram Cell Structure and Peripheral Circuitry

KEYWORDS: SRAM cell, Pre-decoder, Divided word line (DWL), Hierarchical word decoding (HWD), Enable (EN), Control (CTRL).

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ABSTRACT *Memory is the most important building block in rapid development of digital designs as half of the silicon area is used to store data value and program instructions.. The power consumption and speed of SRAMs are important issue that has lead to multiple designs with the purpose of minimizing the power consumption. Bipolar SRAM is faster than that of CMOS SRAM because of small voltage swing on bit-lines also the VBE of bipolar transistor is 0.8 volts, so it requires less time to sense whatever data is stored in the memory. The major constraint of bipolar SRAM is larger power dissipation and complicated control signaling as there is small voltage variation. . CMOS SRAM is preferred over MOS type when large size memory is required, as in CMOS logic there is no static power dissipation. Power is dissipated only in case of change of state in CMOS SRAM. Major portion of memory chip is taken up by cell array, so if cell size can be reduced we can have smaller area. This paper focuses on the read and writes operation of 6t SRAM cell and peripheral circuitry such as row address decoder, column multiplexer, sense amplifier which are main building blocks of SRAM cell. The peripheral circuitry has a tremendous impact on the robustness, performance, and power consumption of the memory unit so careful analysis of the options and consideration of periphery design is appropriate.*

Introduction
Static random-access memory is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered

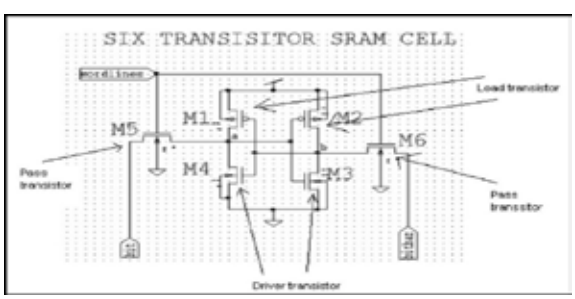

Figure 1

Terminology
Bit lines- Carries complementary data, Word line- used for addressing, Pass transistor- used for accessing

SRAM Sizing
High bit line must not overpower inverters during SRAM read. But low bit lines must write new value into cell [1].

SRAM Operation
Standby Mode (the circuit is idle).

When word line is not asserted (word line=0), the access transistors M5 and M6 disconnect the cell from bit lines. The two cross coupled inverters formed by M1-M4 will continue to reinforce each other as long as they are connected to the supply. So when WL=0, access transistorsM5 and M6 are off and data held in the latch.

Read Mode (the data has been requested).
Assume that 1 is stored at node a. The read cycle is initiated by pre-charging bit-lines to high voltage pulse, and then asserts word line high. Word line enables both the access transistor which will connect cell from the bit lines. The second step occurs when the values stored in a and b are transferred to the bit lines one of the bit line will discharge through the driver transistor and the other bit lines will be pull up through the Load transistors toward VDD, a logical 1[2]. Design of SRAM cell requires read stability (do not disturb data when reading). For read stability node 'a' must not flip and M4>>M5.

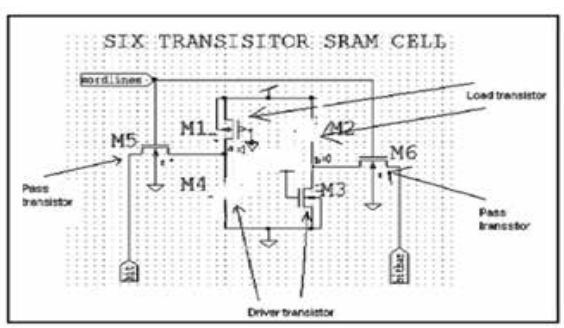

Figure 2
Figure 2 showing read operation in which 1 is stored at node a, 0 is stored at node b.

Write Mode (updating the contents).
Assume that the cell is originally storing a 1and we wish to write a 0. To do this, the bit line is lowered to 0V and bit bar is raised to VDD, and cell is selected by raising the word line to VDD. Typically, each of the inverters is designed so that PMOS and NMOS are matched, thus inverter threshold is kept at VDD/2. If we wish to write 0 at node a, M5 operates in saturation. Initially, its source voltage is 1. Drain terminal of M4 is initially at 1 which is pulled down by M5 because access transistor M5 is stronger than M1. Now M2 turns on and M3 turns off, thus new value has been written which forces bit line lowered to 0V and bit bar to VDD. SRAM to operate in write mode must have write-ability which is minimum bit line voltage required to flip the state of the cell.

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SRAM Peripheral circuitry
Address Decoder
Whenever a memory allows for random address-based access, address decoders must be present. The design of these decoders has a substantial impact on the speed and power consumption of memory. There are two classes of decoders.

1. Static Row Decoder
The task of Row decoder is to enable one memory row out of 2^M row. A 1 out- of- 2^M decoder is nothing less than a collection of 2^M complex, M- input, logic gates. Consider an 8-bit address decoder. Each of the outputs is a logic function of the 8 input address signal (A_0-A_7). The row with address 0 is enabled by the logic functions: WL_0=! A_0&! A_1&! A_2&! A_3&! A_4&! A_5&! A_6&! A_7 ------1. Above function can be implemented in two stages, using a single 8- input NAND gate and an inverter. For a single-stage implementation, it can be transformed into a wide NOR using De-Morgan rule. WL_0=! (A0+ A_1+ A_{2+} A_3+ A_4+ A_5+ A_6+ A_7)

Implementing above function 8 inputs NOR gate per row is required, so number of transistors needed will be 256*(8+8) =4,096. This poses several imposing challenges. First of all, the layout of the wide-NOR must fit within the word line pitch. Secondly, the large fan –in of the gate has a negative impact on performance because of squared dependency between delay and Fan-in. This problem can be solved by splitting a complex gate in to two or more logic layers. This decomposition concept makes it possible to build fast and area-efficient decoders, and is used effectively in most memories. Segments of the address are decoded in a first logic layer called the pre-decoder. A second layer of gates then produces the final word-line signals. So expression 1 can be regrouped in the following way [3]. WL_0=! (! A_0+ A_1) & (! A_2+ A_3) & (! A_4+ A_5) & (! A_6+ A_7)

A NAND decoder using 2- input pre-decoders

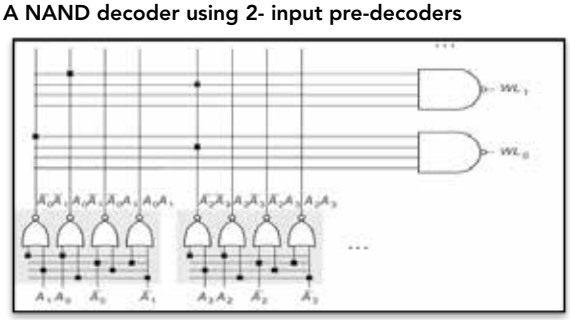


Figure 3

The address is partitioned into section of 2 bits that are decoded in advance. The resulting signals are then combined using 4-input NAND gates to produce the fully decoded array of word- line signals. Pre-decoders reduce number of transistors required. The number of active device in the 8-input decoders equals 256*8+ (4*4*4) =2,112, which is 52% of a single stage decoder, which would require 4,096 transistor. One of the main function of a decode hierarchy to minimize the fan-in of parts of decode circuit because higher fan-in gates have a large Logical effort, making them less efficient. The output of these pre-decoders are then combined by low fan-in gates to produce the final decoder output which are the word line signals connected to the memory cells.

Advantages of Pre-decoding
Pre-decoders results in a smaller, faster, low power circuit.

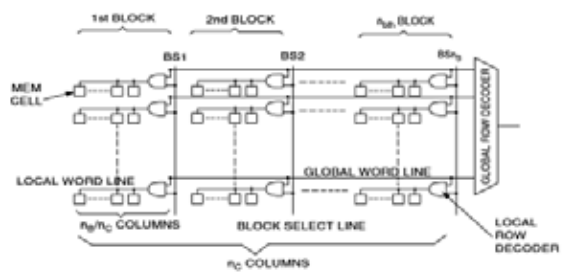
Disadvantages of Pre-decoding
The main disadvantage of Pre-decoding is the need to distribute more wires to propagate all the intermediate pre-decoder outputs, which is minor issue.

Non- partitioned Row decoding
A non-partitioned decode hierarchy refers to a memory organization where all cells in a given row are activated by a single word line output from the row decoder. It is sufficient for very small SRAMs [5].

Advantage
Non- partitioned word line is suitable for very small SRAMs.

Disadvantage
In a non partitioned scheme, every column will have an active memory cell, uselessly discharging the bit-lines of the un-accessed columns and resulting in wasted power needed to pre-charge these bit-lines back to their original value.

Divided Word line (DWL) decoding
DWL involves dividing the memory array along the top-level word line (Global word line) into a fixed number of blocks. Instead of enabling all the cells within a row, the global word line is feed to AND gate with a block-select signal (derived from another subset of the input address) and asserts a local word line (LWL). Only cells connected to this asserted LWL are enabled [5].



An SRAM using the DWL address decoding technique.

Figure 4

Advantage
Since fewer cells are connected to LWL, the power and delay will be significantly less.

Disadvantage
DWL structure is not sufficient to realize the high-speed and low power word decoding as increase of block numbers will result in a large capacitance load on the GWL.

Hierarchical word decoding (HWD)
A logical extension of the DWL scheme is a technique called Hierarchical word decoding (HWD). In this architecture the word line is divided in to three levels; global, sub-global, and local. Though this architecture requires an extra decoding stage, the load capacitance of the global and sub global word lines are reduced compared to the conventional DWL structure.

Advantage
Propagation delay and charging/discharging current of word decoding path are reduced.

Disadvantage
Architecture requires extra decoding stages.

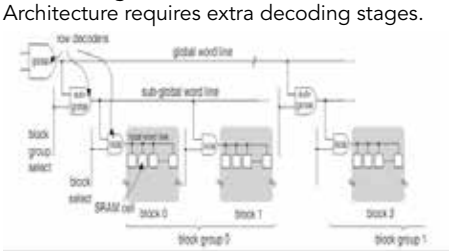


Figure 5

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Hierarchical word decoding(HWD) row decoder
2. Dynamic Row decoder

An M bit row decoder consists of M bit input address lines and 2^M word-lines. For any arbitrary input address combination, only one word line will be selected. The selected row will remain at logic "1" where the other row will get discharged to logic "0".

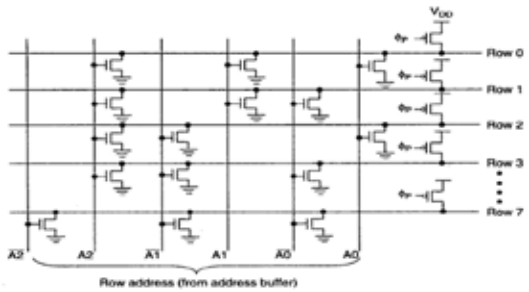

Figure 6

Prior to the decoding process, all word-lines get pre-charged to logic "1". Subsequently, as the address bits and their compliments are applied, the decoding operation commences.

Static v/s Dynamic Decoding
The main differences between the static and dynamic topologies are the speed and the power dissipation. Dynamic is faster while static is more power efficient [6].

Pass transistor based Column decoder/ MUX
Column decoders should match the bit line pitch of the memory array. Column address is decoded and followed by a multiplexer to select column for input or output operation. It requires two outputs to drive complementary pass transistors. Since the requirements for read and write are different column decoder can use separate read and write IO lines. The column decoding is one of the last actions performed in the read sequence, so pre-decoding can be executed in parallel with other operations, and can be performed as soon as the column address is available.

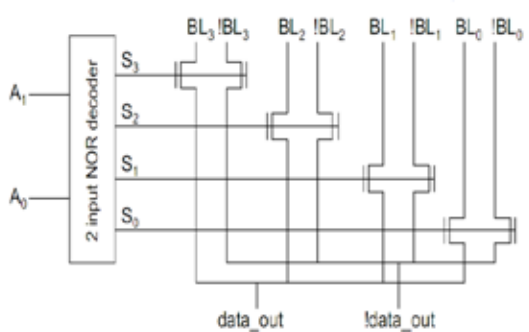

Figure 7

Advantage
Faster since there is only one transistor in the signal path so delay is reduced.

Disadvantage
Large transistor counts.

Tree based Column decoder

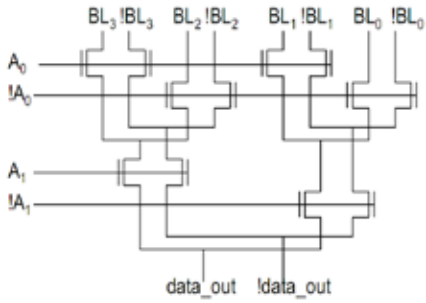

Figure 8

Advantage
Less number of transistors is required.

Disadvantage
Delay increases with the number of section.

Sense Amplifier
Sense amplifier is part of the read circuitry which is used when data is read from the chip. . Column decoder selects one of the sense amplifier, the job of a sense amplifier is to sense the logic levels from a bit-line which represents a data bit (a 1or 0) stored in a memory cell on the chip, and amplify the small voltage swing to normal CMOS logic levels so the data can be output from the chip [6], number of sense amplifier is equal to number of columns and it is used in read condition. If bit line> bit line bar, output is 1 but if bit line bar> bit line, output is 0. During read operation output corresponds to the selected sense amplifier. Sense amplifier allows output to be set quickly without fully charging/discharging bit lines.

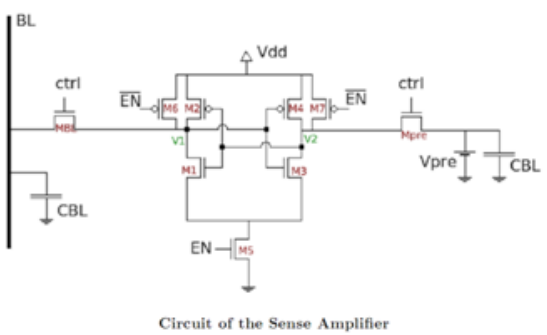

Figure 9
To enable the sense amplifier, the signal EN is set high. The right node (V_2) is pre-charged to a reference voltage. . When CTRL=1 and at the same moment, the left node (V_1) is connected to the bit-line. As soon as CTRL=0, the sense amplifier can start to compare the voltage on V_1 to the reference. If there was "1" written in the SRAM cell, the voltage on V_1 will be higher than reference voltage [6].

REFERENCE 1. Andrei Pavlov Manoj Sachdev, CMOS SRAM Circuit Design and parametric test in nano-scaled technologies | 2. Sedra & smith, Microelectronic circuits, oxford university press, fifth edition, 2004 | 3. Jan M Rabaey & Anantha Chandrakasan & Borivoje Nikolic, Digital integrated circuits-a design perspective, Pearson education, third edition, 2005 | 4. Sung Mo Kang and Yusuf Leblebici, CMOS digital integrated circuits-analysis and design, Tata McGraw hill, third edition, 2003 | 5. Bruce Jacob, Spence& W.NG, David T. Wang, Memory systems. Cache, DRAM, DISK | 6.Users.telenet.be/./verslag_SRAM_Users.telenet.be/./verslag_SRAM_volkaerts_raes_tytgat_vanspav