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A ZVS Interleaved Boost AC/DC Converter With Reduction in Switching Losses

KEYWORDS

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ABSTRACT *Modern AC-DC power supplies utilize power factor correction in order to minimize the harmonics in the input current drawn from the utility. The Boost topology is the most popular topology for power factor correction today but it has some disadvantages like very high EMI due to reverse recovery of the boost diode and high switching losses caused by hard switching of the boost switch. Many variations of the original boost topology have been suggested to overcome these problems. The Zero Voltage Transition Boost converter is one such solution. In such a converter an auxiliary resonant circuit is employed which is activated only when the boost switch is turning on or off. This auxi1iary circuit allows the boost switch to turn on and off under zero voltage conditions thus reducing the switching losses. In this paper a soft-switching boost power converter is proposed and analyzed.*

1. INTRODUCTION

In modem power applications a reliable ac-dc power converter is required. For power applications above 250 W, a two stage process is usually used to provide an isolated and regulated dc output voltage. The first stage of such a converter is a rectifying stage that converts the ac voltage to dc and the second stage is an isolated dc-dc converter that converts the dc input voltage into a regulated dc voltage at the output. One of the most important functions of the rectifying stage is to provide Power Factor Correction (PFC) of the input current in order to minimise the harmonics in it.

Historically diode bridge rectifiers with a large capacitor at the dc bus have been used to convert the ac voltage to a dc voltage. But diode bridge rectifiers draw a very high peak current from the ac utility which is rich in harmonics and thus gives a very poor power factor of about 0.6. International standards such IEC 61000 and IEEE 5 19-92 lay down the maximum amount of harmonics that can be tolerated in the system and diode bridge rectifiers cannot match these criteria. Many topologies such as Buck, Boost, Single Stage converters etc. can be used for PFC applications to overcome these problems. The filtered input current in most of these topologies resembles closely giving a power factor close to unity.

1.1PWM Boost Converter for PFC applications

The switch mode boost converters can perform power factor correction by shaping the input current to be sinusoidal and forcing it to follow the input voltage waveform. This achieves a power factor close to unity and the harmonics are also reduced. However boost converters suffer from their own set of disadvantages:

1) The output of a boost converter is always greater than the peak input voltage. So if a converter is designed for Universal Input Line Applications the output dc bus voltage must be greater than the peak of the 265 Volt ac wave. Thus the output voltage of the boost must be kept at least 400 V and turning on the main switch of the converter at such a high voltage causes a lot of turn-on losses in the switch.
2) The boost switch has hard turn-on as well as hard turn-off and the boost diode has a hard turn-off. This causes additional losses. During the reverse recovery of the boost diode the output capacitor is shorted to ground and this causes a very large and negative current spike to appear in the converter switching waveforms. This current spike causes a large amount of EMI in the circuit and can cause problems in telecommunication systems.

Thus a converter which can minimise these switching losses and reduce the EMI is required. The losses can be substantially reduced by using soft switching techniques

1.2 How to reduce Hard Switching Losses

As there are f_s such as turn-on and turn-off transitions during each switching cycle then the switching loss in the switch given in [1] shall be:

$$P_s = \frac{V_0 I_0 f_s}{2}(t_{on} + t_{off})$$

This equation shows that the switching loss in any semiconductor switch varies linearly with switching frequency f_s and the delay times. Such a switch mode converter is therefore unsuitable for operation at high frequencies above 20 W. Although switching stresses can be reduced by using simple dissipative snubbers across the switch the efficiency of the converter is not improved as the switching power loss shifts from the switch to the snubbers.

From the above equation an important result can be deduced that switching losses can be reduced by two methods:

1) By reducing the turn-on and turn-off delay times. This is done by using faster and more efficient switches in the converter.
2) By making the current or voltage across the switch zero before turning it on or off. Soft switching resonant converters are based on this concept.

2. MODES OF OPERATION OF CONVERTER

Fig. 1 shows the power circuit of the ZVS interleaved boost PFC converter. In this converter, two boost converters operate with 180^0 phase shift in order to reduce the input current ripple of the converter. This 180^0 phase shift can be used to provide reactive current for realizing ZVS

Volume : 4 | Issue : 10 | October 2014 | ISSN - 2249-555X

for power MOSFETs. This auxiliary circuit consists of a HF inductor and a dc-blocking capacitor. Since there may be a slight difference between the duty ratios of the two phases, this dc-blocking capacitor is necessary to eliminate any dc current arising from the mismatch of the duty ratios of the main switches in the practical circuit.

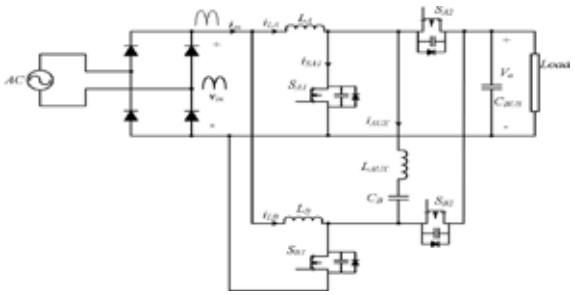

Fig.1: Proposed ZVS interleaved boost PFC schematic

Fig. 2 shows the key waveforms of the converter for D<0.5. According to this figure, there are eight operating modes in one switching cycle of the converter. The operating modes are explained as follows.

2.1 Mode I ($t_0 < t < t_1$)
This mode starts when the gate pulse is applied to SA1. Once the voltage is applied to the gate, SA1 is turned ON under zero voltage. Since SA1 and SB1 are ON during this interval, the voltage across the auxiliary inductor is zero.

2.2 Mode II ($t_1 < t < t_2$)
This mode is the dead time between the phase B MOSFETs. During this interval, the auxiliary circuit current charges the output capacitance of SB1 and discharges the output capacitance of SB2. In this mode, the average voltage across the boost inductance L_B is zero.

2.3 Mode III ($t_2 < t < t_3$)
Once the output capacitors of SB1 and SB2 have been charged and discharged completely, the gate signal of SB2 is applied and SB2 is turned ON under ZVS. During this interval, the voltage across the auxiliary circuit is –Vo.

2.4 Mode IV ($t_3 < t < t_4$)
During this mode, the output capacitor of SB2 is charging from zero to Vo and the output capacitor of SB1 is discharging from Vo to zero. This period is actually the dead time between SB2 and SB1.

2.5 Mode V ($t_4 < t < t_5$)
This mode starts when the gate signal is applied to SB1 .Once the gate has been applied, SB1 is turned ON under ZVS. Since SA1 and SB1 are ON during this period, the voltage across the auxiliary inductor is zero; hence, the auxiliary inductor current remains constant at its peak value.

2.6 Mode VI ($t_5 < t < t_6$)
During this mode, the output capacitor of SA1 is charging from zero to V_0 and the output capacitor of SA2 is discharging from V_0 to zero. This period is also the dead time between SA1 and SA2.

2.7 Mode VII ($t_6 < t < t_7$)
During this mode, the voltage across the auxiliary circuit is V_0. SA2 is conducting the current to the output.

2.8 Mode VIII ($t_7 < t < t_8$)
During this mode, the output capacitor of SA1 is discharging from V_0 to zero and the output capacitor of SA2 is charging from zero to V_0. In this mode, the current through L_A is at its minimum value I_V and the excess current from the auxiliary circuit charges and discharges the output capacitors.

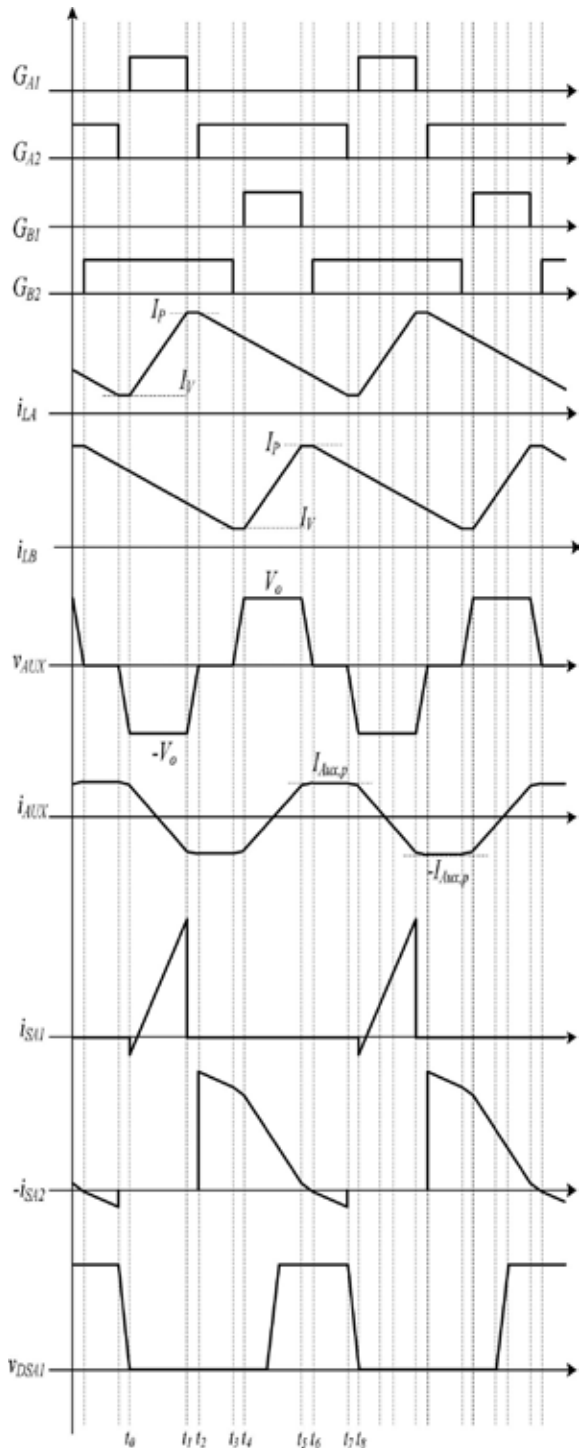

Fig.2: Key Waveforms for D < 0.5

3. SIMULATION DIAGRAM
The topology is designed using simulink tool of MATLAB and simulation was done. The model is shown below in Fig.3.

Volume : 4 | Issue : 10 | October 2014 | ISSN - 2249-555X

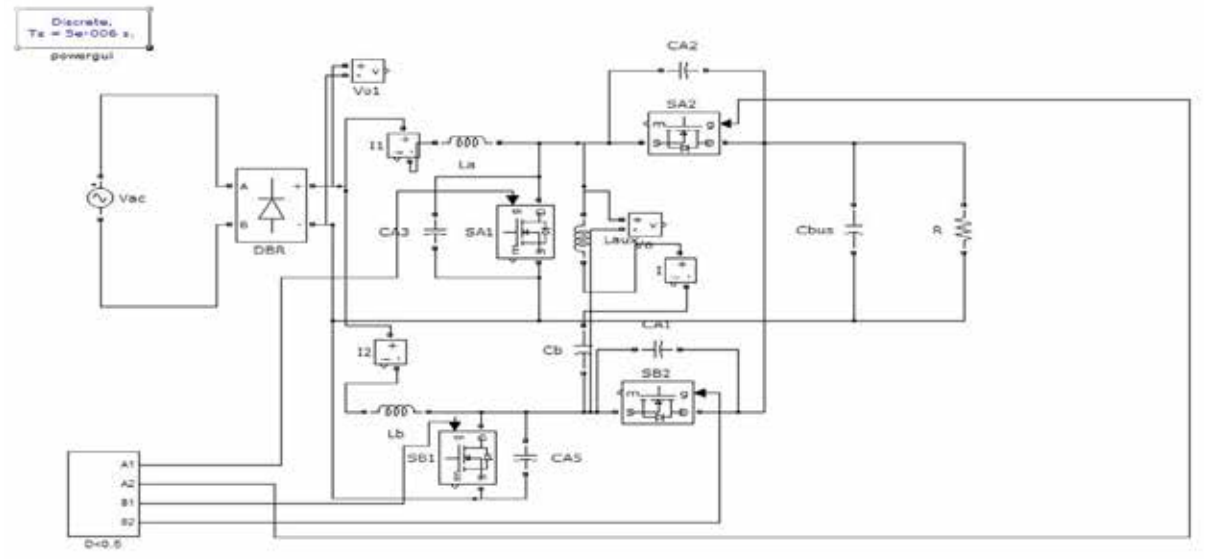

Fig.3: Simualtion Diagram

4. SIMULATION RESULTS

Some of the key waveforms obtained after simulation is given as follows. The gating pulses for the four MOSFETs with duty ratio less than 0.5 were used. The inductors connected in each phase limits the current and that can be seen as the sharp rise and fall of the voltages. The current and voltages across the passive auxiliary circuit is shown. A sharp rise in both the current and voltage waveforms are observed. The waveform of switch SA1shows us clearly that the ZVS is achieved.

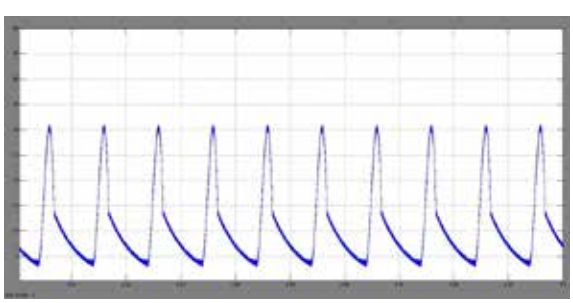

Fig.4: Inductor A Current

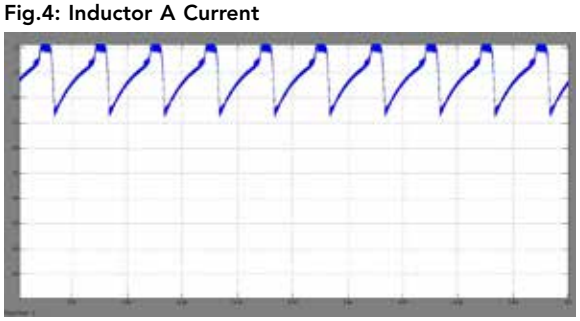

Fig.5: Inductor B Current

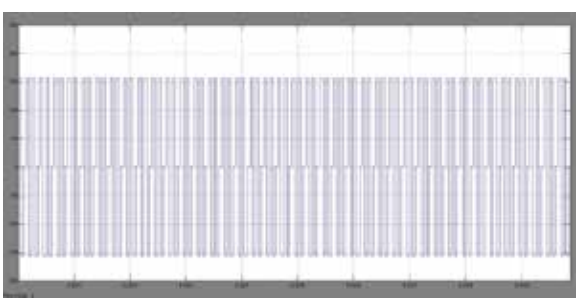

Fig.6: Auxiliary Circuit Voltage

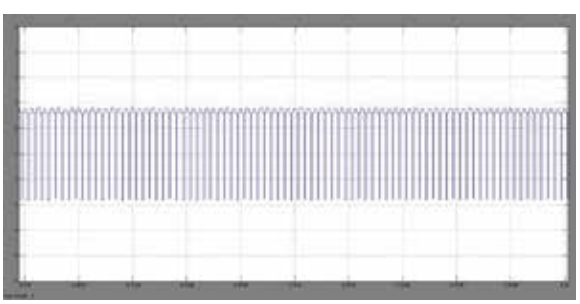

Fig.7: Auxiliary Circuit Current

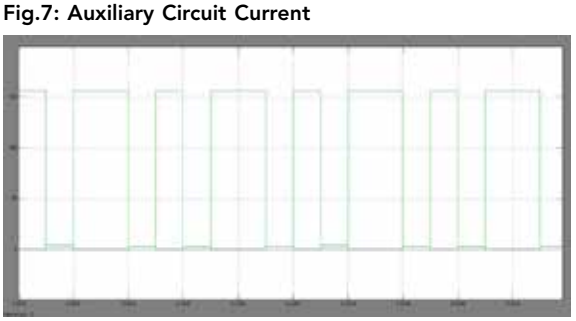

Fig.8: Current & Voltage of Switch SA1

5. CONCLUSION

A new interleaved boost PFC converter is proposed, which provides soft switching for the power MOSFETs, through an auxiliary circuit. This auxiliary circuit provides reactive current during the transition times of the MOSFETs to

Volume : 4 | Issue : 10 | October 2014 | ISSN - 2249-555X

charge and discharge the output capacitors of the MOSFETs. In addition, the control system effectively optimizes the amount of reactive current required to achieve ZVS for the power MOSFETs. The frequency loop, which is introduced in the control system, determines the frequency of the modulator based on the load condition and the duty cycle of the converter. The experimental results and efficiency curves show the superior performance of the proposed converter compared to the conventional one.

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