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A Microprocessor System for Cheese Quality Evaluation by Hyperspectral Images

KEYWORDS: microprocessor system, hyperspectral images, cheese quality

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ABSTRACT *The paper reports on the development of a microprocessor system base on digital media processor TMS320DM6437 for cheese quality evaluation by hyperspectral images processing. The presented microprocessor system captures hyperspectral sliced images and makes images processing. The diagram of the microprocessor system, hardware structure description, algorithm description for preprocessing by wavelet transformations and quality features reduction are given. Quality features reduction is made by sequential forward selection algorithm. Experiments show that the microprocessor system has a good performance for objective quality evaluation of cheese products.*

INTRODUCTION

Acquisition and processing of hyperspectral images is a new promising technology successfully combines the advantages of computer vision and spectroscopy methods for modern objective contactless quality food evaluation. Hyperspectral technology is a contactless nondestructive, requires no pre-treatment of samples obtained both spatial and spectral information for samples allows a more complete description of the constituent concentration and distribution in heterogeneous foods as cheese. Hyperspectral technology is very sensitive to detect small components in the cheese and allows examination of samples with different geometries. Processing of hyperspectral images of cheese requires fast image processing hardware. Many authors report that they use hyperspectral images for food evaluation, but they have not published details of their computer systems for processing [4]. The goal of this paper to report a microprocessor system for cheese quality evaluation by hyperspectral images processing.

The author designs a full working microprocessor system and implements algorithms for preprocessing and features selection for cheese assessment. The author uses a new kind of digital media processor (**DMP**) for his proposed microprocessor system, because modern **DMP**s are flexible and suitable to extremely complex math intensive tasks such as hyperspectral image processing. The presented system is suitable for testing and grading for all types of cheese by conveyer stepper moving. Some basic algorithms are developed for system performance tests, because we know that microprocessor are useless without software [3].

COMPONENTS DIAGRAM OF COMPUTER PLATFORM FOR CHEESE QUALITY EVALUATION

Analyzing the principles of obtaining possible hyperspectral images by relatively not-admitting the light turbid non-homogenous object with predominant reflected flow of light, for quality grading of cheese products the system has to be with zone incremental linear scanning (Fig.1)

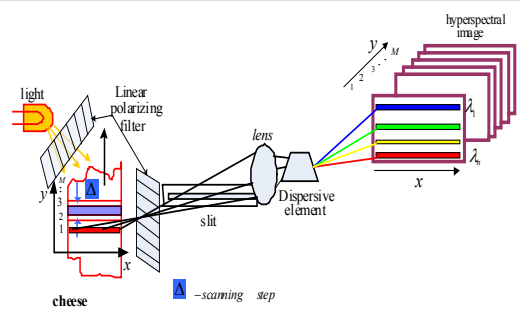

Figure 1: System of incremental scanning of cheese

The scanning system enables regulation of the speed of processing by changing the scanning increment through adaptive feedback. Considering the details of the different scanning systems for obtaining hyperspectral images is possible to synthesize modern model of computer platform for objective non-destructive quality assessment of cheese by processing hyperspectral images. Computer platform for determining the quality characteristics of cheese consist of interconnection hardware and software components.

A model design diagram of computer platform for cheese quality evaluation is given in Fig.2.

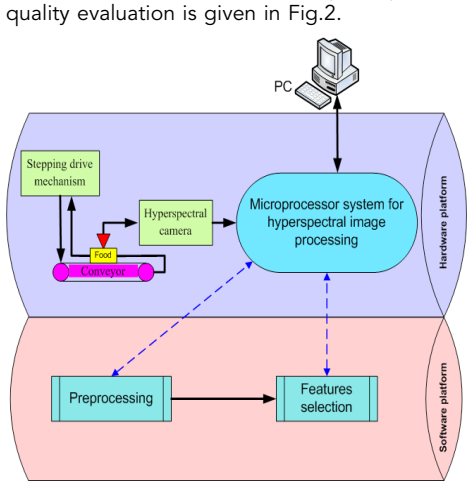

Figure 2: Design diagram of the computer platform

Presented model of the computer platform in Fig.2 shows that the hardware platform consists of stepping drive mechanism, conveyor, hyperspectral camera and microprocessor system for hyperspectral image processing.

This paper highlights subsystems making hyperspectral image processing. Hardware subsystem (microprocessor system for hyperspectral image processing) consists of a high performance DMP for image processing. Software subsystem is divided into algorithmic modules (preprocessing and features selection) according to the tasks performed by the software associated with the preprocessing hyperspectral images and reduction of feature space.

DESIGN OF THE MICROPROCESSOR SYSTEM

Hardware Structure

Diagram of the designed microprocessor system for cheese quality evaluation is given in Fig.3. The author uses the high performance **DMP** chip TMS320DM6437 of Texas Instrument (**TI**) as a core, design and realizes a whole hardware subsystem. The TMS320DM6437 offers cost-effective solutions to high-performance DSP programming challenges with up to 5600 MIPS at a clock rate of 700 MHz. The core processor has 64 general-purpose registers of 32-bit word length, two multipliers for a 32-bit result and six arithmetic logic units (**ALUs**). The DM6437 core uses a two-level cache-based architecture. The Level 1 program memory/cache (**L1P**) consists of a 256K-bit memory space that can be configured as mapped memory or direct mapped cache, and the Level 1 data (**L1D**) consists of a 640K-bit memory space, 384K-bit of which is mapped memory and 256K-bit of which can be configured as mapped memory or 2-way set-associative cache. The Level 2 memory/cache (**L2**) consists of a 1M-bit memory space that is shared between program and data space. **L2** memory can be configured as mapped memory, cache, or combinations of the two. The DM6437 device includes a Video Processing Subsystem (**VPSS**) with two configurable video/imaging peripherals: one Video Processing Front-End (**VPFE**) input used for video capture, one Video Processing Back-End (VPBE) output.

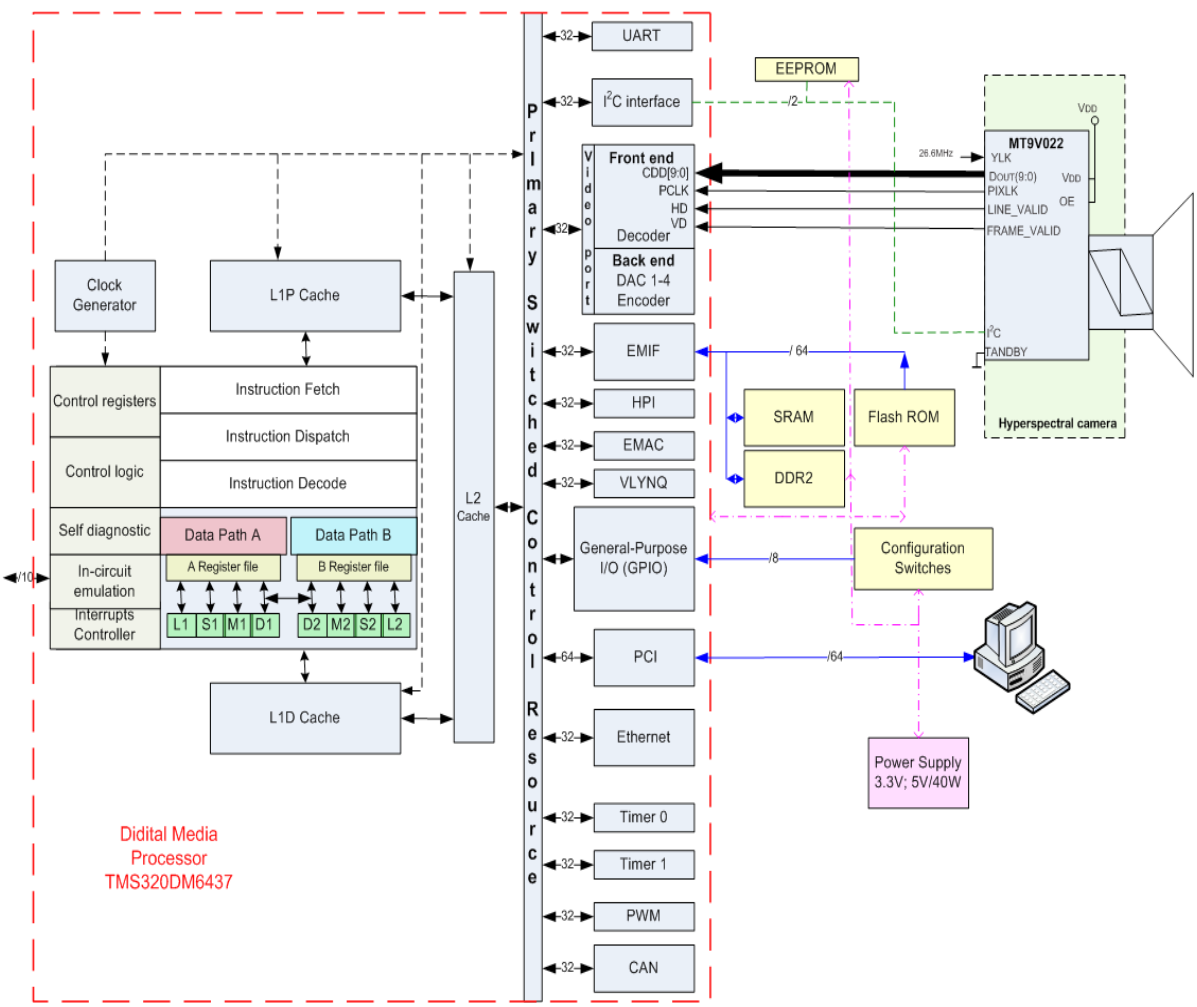

Figure 3: Diagram of the microprocessor system

The peripheral set includes: two configurable video ports; a 10/100 Mb/s Ethernet MAC (EMAC) with a management data input/output (MDIO) module; a 4-bit transmit, 4-bit receive VLYNQ interface; an inter-integrated circuit (I^2C) Bus interface; two multichannel buffered serial ports (McBSPs); a multichannel audio serial port (McASP0) with 4 serializers; two 64-bit general-purpose timers each configurable as two independent 32-bit timers; one 64-bit watchdog timer; a user-configurable 16-bit host-port interface (HPI); up to 111-pins of general-purpose input/output (GPIO) with programmable interrupt/event generation modes, multiplexed with other peripherals; two UARTs with hardware handshaking

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support on one UART; 3 pulse width modulator (PWM) peripherals; one high-end controller area network (CAN) controller; one peripheral component interconnect (PCI); and two glueless external memory interfaces: an asynchronous external memory interface (EMIFA) for slower memories/peripherals, and a higher speed synchronous memory interface for DDR2 [5]. The microprocessor system has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. The given system incorporates a 64 bit wide external memory interface. Addresses are always 32-bits wide. By default, the internal memory sets at the beginning of the address space. The EMIF (External Memory Interface) used to serve external memory. The external memories of system consist of a 128 Mbytes of DDR2 SDRAM, 16 Mbytes of non-volatile Flash memory and 2 Mbytes SRAM. DDR2 is used for program, data, and video storage. Memory refresh for DDR2 is handled automatically by the TMS320DM6437. The microprocessor system has a two configuration switches to control the operational state of the processor. The microprocessor system incorporates an I2C EEPROM with capacity of 1MB for booting purpose. The TMS320DM6437 has an internal PLL which can multiply the input clock to generate the internal clock.

The MT9V022 image sensor was chosen for hyperspectral camera due to its suitability for hyperspectral imaging, because it can be used in the wavelength range from 300 nm to 1100 nm of the spectrum. The image sensor provides a resolution of 10 bits per pixel, is able to capture both continuous video and single frames progressively. All image sensor registers are written and read through the I^2C serial interface. The I^2C address of the MT9V022 is fixed and consists of seven bits of address and 1-bit of read/write direction. Full registers descriptions are given in datasheet of MT9V022 [1]. The image sensor interfaced to the microprocessor system through the video port processing front end (VPFE) of TMS320DM6437. The FRAME_VALID signal on the MT9V022 is connected to VD signal on the TMS320DM6437 which can take advantage of this signal. However, the FRAME_VALID line is not needed since the information necessary for proper operation with the TMS320DM6437 is carried on the LINE_VALID signal. Recall that the LINE_VALID and FRAME_VALID signals indicate that a line and frame of valid pixel data is available on the data bus. Because the TMS320DM6437 samples data when HD is active, proper video port and MT9V022 operation requires that the LINE_VALID signal to be connected to the HD signal.

Software Structure

Preprocessing

The hyperspectral images of cheese taken down in steps constitute two-dimensional images subdivided in subspaces by using multiple-resolution approximation of the initial space into low-frequency components – constituting optimum approximation and into high-frequency components constituting detailed information of the original signal [2]. The decomposition coefficients in the wavelet orthogonal basis are divided by:

$$c_{j;k,l} = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} h_{m-2k} h_{n-2l} c_{j-1;m,n} \quad (1)$$

$$d^1_{j;k,l} = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} h_{m-2k} g_{n-2l} c_{j-1;m,n} \quad (2)$$

$$d^2_{j;k,l} = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} g_{m-2k} h_{n-2l} c_{j-1;m,n} \quad (3)$$

$$d^3_{j;k,l} = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} g_{m-2k} g_{n-2l} c_{j-1;m,n} \quad (4)$$

, where tc_j are approximation coefficients, d_j are the detailing coefficients.

The sequence H={h_k | k=…,-2,-1,0,1,2,…} is designated as a scaling filter.

The sequence G={g_k | k=…,-2,-1,0,1,2,…} is designated as a wavelet filter.

For Haar wavelet $h_0 = 1/\sqrt{2}$, $h_1 = 1/\sqrt{2}$, $g_0 = 1/\sqrt{2}$ и $g_1 = 1/\sqrt{2}$.

The process of dual-scale approximation is illustrated in Fig. 4.

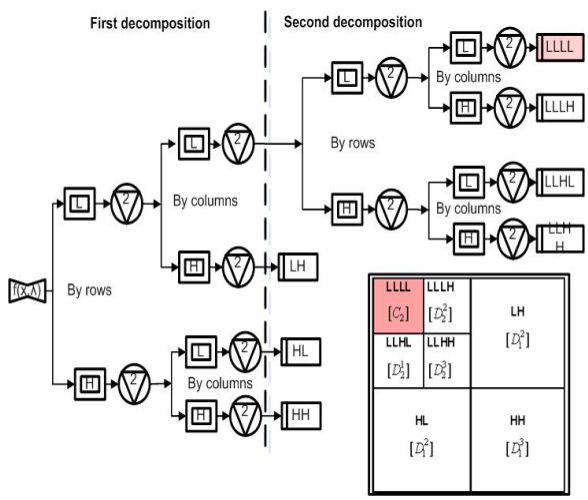

Figure 4: Diagram of two levels transform of sliced hyperspectral image

The filters divide the input signal into frequency bands. The filtered signals at the exit of the filters are obtained with double length, so after the filtration decimation is performed, i.e. removal of all odd coefficients. The high-frequency filter (H) is related to $\psi(t)$, while the low-frequency filter (**L**) is related to $\phi(t)$. The processing of images f(x,λ) with a array of dimensionality (**N**,**M**) is performed separately by rows and columns, by first performing **1-D** convolution with coefficients $h_0(k)$ /low-frequency filter L/ and $h_1(k)$ /high-frequency filter H/. After that follows a decimation with a factor 2 i.e. a new array is obtained (**N**/2, **M**). Upon processing by columns also **1-D** convolution $h_0(k)$ (low-frequency filter L) is applied and $h_1(k)$ (high-frequency filter **H**) and then decimation with a factor 2. Thus a single high-scale approximation is performed. As approximating coefficients C_1 are in a matrix form with dimensionality (**N**/2), **M**/2). It is possible to apply for a second time high-scale approximation on the matrix with approximation coefficients whereby a new reduction of the feature space is obtained up to approximation coefficients C_2.

Feature spaces reduction by sequential forward selection /SFS/

The sequential forward selection /**SFS**/ method begins the evaluation from the most informative feature and at each level one additional feature is added, which in combination with the already selected ones maximizes the target function. Fig. 5 shows how this method performs the selection.

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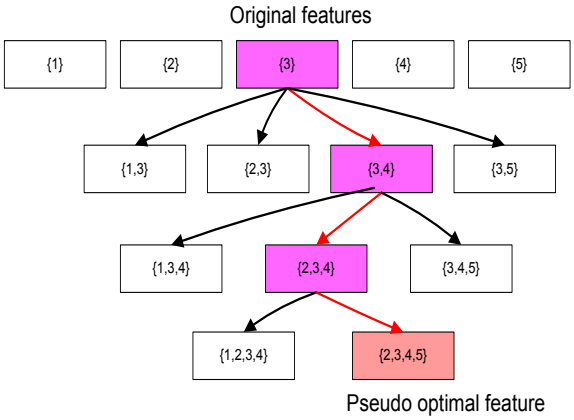

Figure 5: Method of the sequential forward selection

Once a given feature is selected, it cannot be removed. Since this method does not analyze all possible cases, here it is relied that the range of informative features will also give a good combination. In practice, however, the so-called problem of the nest can appear, i.e. to omit the appropriate combination of aggregate features.

In the elaboration a new modified algorithm is used, presented as a pseudo code below:

1. F={0}

2. Select the best feature

$$\varphi^{+} = \arg\max_{\phi \notin F_m} J(F_m + \phi)$$

$F_m = F_m + \phi^{+}$; m=m+1

3. Select the worst feature

$$\varphi^{-} = \arg\max_{\phi \in F_m} J(F_m - \phi)$$

4. If $J(F_m - \phi^{-}) > J(F_m)$ then m=m+1 and go to step **3**,

else go to step **2**.

Bhattacharyya distance is used as criteria function for features selection:

$$J = \frac{1}{8}(\mu_i - \mu_j)^T \left(\frac{C_i + C_j}{2}\right)^{-1} (\mu_i - \mu_j) + \frac{1}{2}\ln \left| \frac{\frac{C_i + C_j}{2}}{\sqrt{|C_i||C_j|}} \right|, \quad (5)$$

where μ_i, μ_j and C_i, C_j are the mean vector and covariance matrix of class i and j respectively. For 3-classes problems, the average of all class-pair distance is calculated as the criterion value. The spectral characteristics of cheese obtained from the sensor block are analyzed and classified successively band by band, pixel by pixel, by being grouped into three classes: K1-caseins, K2-fats and K3-contaminations.

An algorithm for determining the quality of cheese products based on the processing of hyperspectral characteristics is shown in Fig. 6.

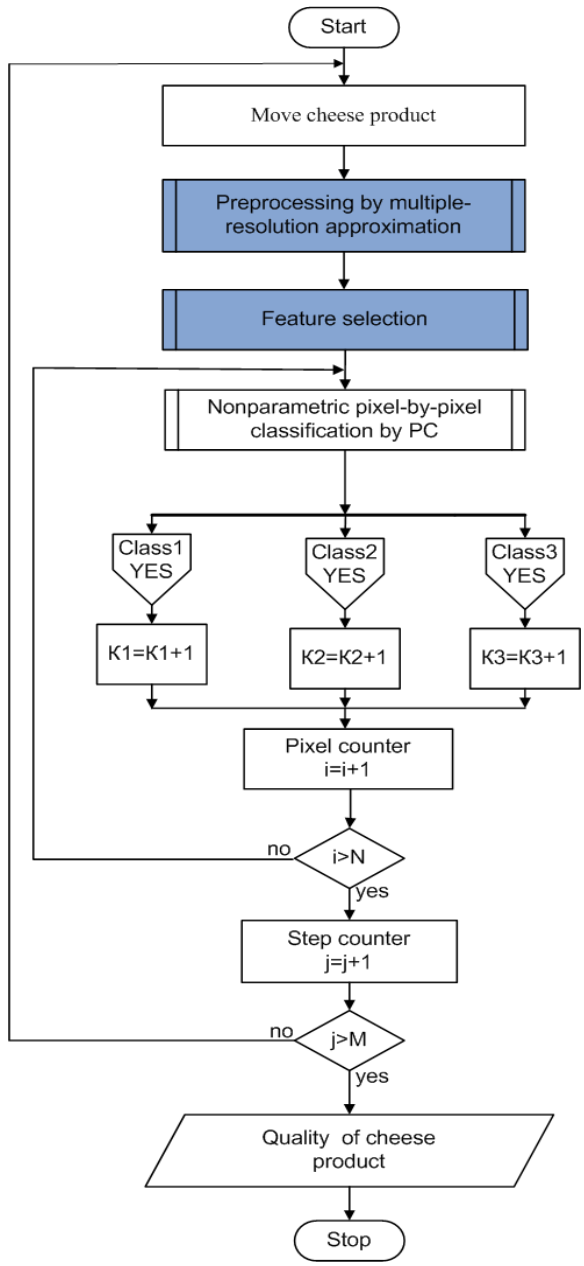

Figure 6: Algorithmic structure for objective quality grading of cheese

C. Testing of the System

The development test of the proposed microprocessor system was made by JTAG emulator XDS560 connected between TMS320DM6437 and personal computer ASUS M51AC i7. The performance of data processing is tested with 320x240 pixel images from hyperspectral camera CMOS sensor. In the experiment 20 linearly scanned hyperspectral images of Bulgarian cow white cheese product were used. The algorithms are realized in C program environment for digital signal processor TMS320DM6437 of Texas Instruments. The analysis of the video signal is line oriented. Table 1 shows the results obtained per time for machine processing for one step of scanning /one slice/ for each of the algorithms realized upon fixed six features of reduction.

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TABLE 1
VALUES OF PROCESSING TIME IN PROPOSED MICRO-PROCESSOR SYSTEM

Algorithms	Machines cycles	Processing Time Value [s]
Initialization	3418	$5.696*10^{-6}$
Preprocessing	143868544	0.23978
Features selection	2137612425	3.56268
Total:	2281484387	3.80246

The actual power consumption in this experiment with proposed microprocessor system based on TMS320DM6437 is 6.1 W. The total maximum power consumption of all components of the microprocessor system is less than 8 W, according to component manufacturers.

CONCLUSIONS

The performance test result shows that this microprocessor system has total processing time under 76.05 seconds per 20 slides quality tracking. This system could be applied to build computer platform for cheese food evaluation by hyperspectral image processing. The proposed microprocessor system based on high performance video signal processor TMS320DM6437 has small size, power consummation under 8 W and can use as mobile quality evaluation platform on production lines and shops. An innovative microprocessor system for cheese quality evaluation is show in this paper.

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