RESEARCH PAPER | Engineering | Volume : 5 | Issue : 2 | Feb 2015 | ISSN - 2249-555X

Comparison of Lower Power Vlsi Using Clocked Gate Style And Non-Clocked Style

KEYWORDS: clock gating, lower power VLSI, non clock gating, merge and split, dynamic power wastage, half adder.

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ABSTRACT *In present world VLSI technology energy consumption is an important factor to be considered among other factors like area occupation,performance and speed of the portable devices. The reduction in size and complexity of the portable devices have resulted in very large amount of power wastage in the devices .Due to this pneumonia low power VLSI designs have become very important part of portable devices. There is more strategy for designing the lower power VLSI. In this paper I have compared only 2 methods of designing the lower power VLSI using clocked logic style and non-clocked logic style. It minimizes the power wastage by controlling the clock whenever the clock is not used. Merge and Split concepts were applied in clocked gating style design to reduce power wastage. Experimental output show that these designs achieves low power wastage. In non-clocked logic style different method are compared by testing transistor level simulations for half adder circuit using Eldo simulator of Mentor graphics.*

1. INTRODUCTION:

Now a days power energy wastage is an important factor to be considered among other factors like speed and performance. As there is more advancement in technology, it gives a development of portable devices which are smaller in size and more complex in design. As we go for complex design and smaller size power wastage is more. So that low power designs have become very important part of portable devices. The important effect of power wastage is the heat produced from the device. As the temperature increases life time of the transistor decreases. This affects the performance of the devices.

The increasing demands on low-power VLSI can be separated at different design levels, like circuit design, layout, and the process technology level. So that more methods are used to design low power VLSI. I have compared two methods one is clocked logic and another method is non-clocked logic styles which are used as architectural designing of low power VLSI. In clocked logic method merge and split method is used to design a lower power VLSI.

2. CLOCKED LOGIC TECHNIQUE:

Clock gate technique is a technique where the part of design is gated. In this technique the power consumption by reducing the storage of same bit to memory of the flip-flop . In different methods the this technique were used to a design, system level, sequential clock gating and combinational clock gating.

In system level clock gating, design can be gated when not in use. For example when the mobile is in ideal state for few second it automatically switch off the display like this way we can reduce the power consumption. In sequential clock gating the clock used in the flip-flop in a pipelined design were switched off when the clock is not in use. This type of clock logic gate method is difficult to provide the capability to implement it in the feature so we have to verify the result which is very difficult to achieve.

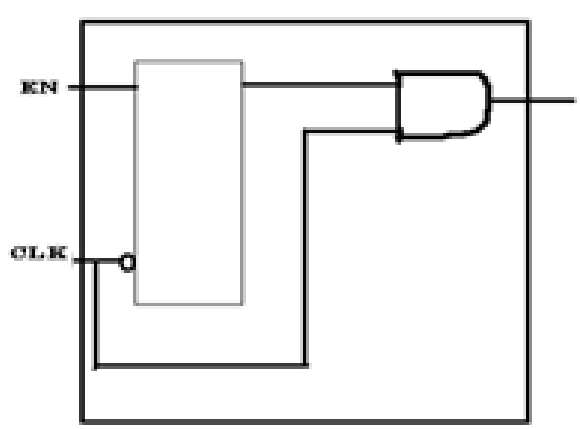

Figure1:clock gate with latch

Volume : 5 | Issue : 2 | Feb 2015 | ISSN - 2249-555X

3. CLOCK TREE SYNTHESIS:

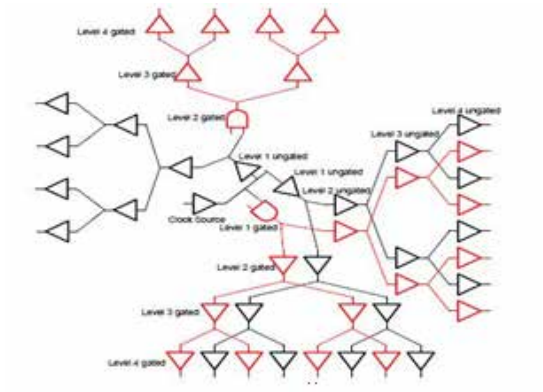

Figure2:structure of clock tree

The clock pulses starts from PLL and it reaches the flip-flop and other sequential elements. The travelling path of the clock signal to reach the flip-flop is known as clock tree. It branches to a number of sequential elements present in a tree. The clock pulse which starts from PLL source does not reaches the flip-flop at same time. Figure2 shows the structure of clock tree. Synthesis of the tree is the process the clock signals are buffered to the sequential elements so that they reaches the flip-flop at the same time.

The report gives the structure of clock tree and phase delay for different in a design. We can compare both timing and power between gated design and ungated in a design.

4. IMPLEMENTATION OF CLOCK GATE:

Implementation of design in RTL compiler and the low power tools are invoked. The code generated in VHDL are given as the input to RTL compiler by using TCL scripting. The technology files which uses the standard cell library are linked to calculate the power and delay of the design.

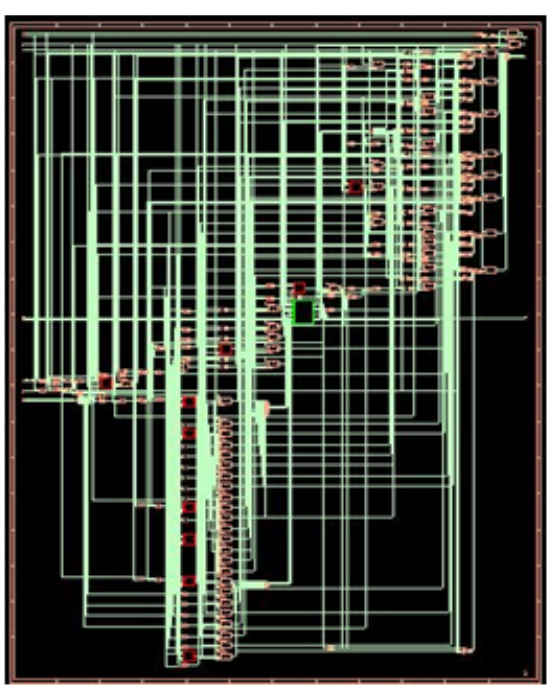

Figure3: Netlist for I2C controller (split)

The elaboration of the design is done from the model to the sub model used in the design. Both technology and generic mapping are done and the results are taken from it. Split and merge of clock gating cells are performed using the rc- script window, and netlist and sdc files are taken from the rc script window. Figure3 and figure4 shows the netlist schematic for I2C controller.

The files which are taken from the rc scrpit window were given as the input to soc encounter for getting the timing information and clock tree structure.

Inputs for clock tree are given such that inverters and clock buffers to be used for generating the structure of the clock tree. Synthesis of the tree report gives the information about the number of flip-flops, sub-tree, skew and clock buffer.

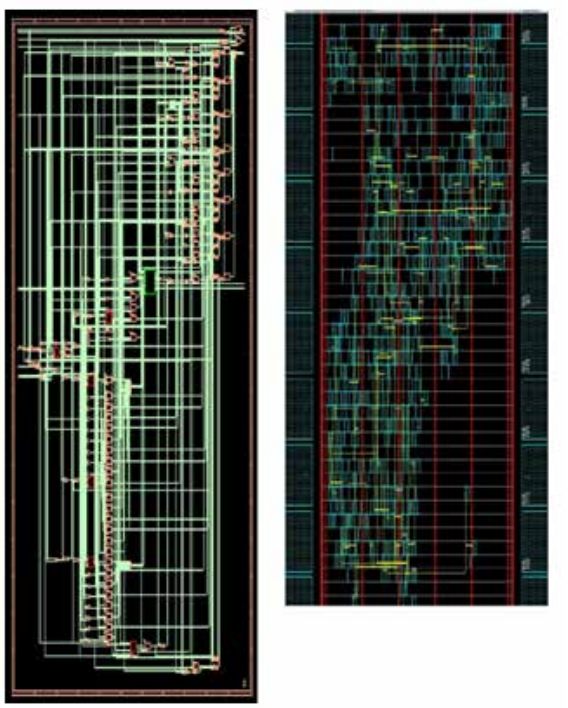

Figure4: Netlist for I2C controller (merge)and tree structure for gated I2C (split).

5. SPLIT AND MEARGE METHOD:

From the structure of clock tree we can see the report of clock synthesis, the report taken from the clock tree structure gives the information about the slack and skew in the clock distribution network. From the usage of the merge and split techniques appropriately the power wastage and consumption can be reduced. Split is the technique by which the clock gating instances are divided among a fixed number of group of flip-flops. Merge is the process by which flip-flops in the gates at the same time ther are merged under a common clock gating instance.

TABLE-1
RESULT FOR MERGE AND SPLIT DESIGN

	SPLITING	MERGING
AREA	150016	145976
CELLS	771	720
DYANAMIC POWER	132293051.98 (nW)	127975159.581(nW)

Volume : 5 | Issue : 2 | Feb 2015 | ISSN - 2249-555X

	SPLITING	MERGING
TOTAL POWER	132293102.67(nW)	127975209.166(nW)
TIMING SLACK	-917ps	-833ps
RISE SKEW	143.4ps	196.7ps
FALL SKEW	155.8ps	247.9ps

6. Non clocked logic gate:
Non-clocked logic were found everywhere in electronic design, due to a number of opinions including:

- Low power consumption
- Straightforward delay rule timing
- Inherent reliability and noise immunity
- Process variation and defect tolerance etc.

In general, non clocked circuits are quite reliable. Stable nodes finds the value of stages which are successfully given out and provids the noise immunity. Careful device selection gives PFET/NFET device tuning the ratio to achieve required switch and unity gain points for specific noise. In this method defects and process variation does not affect the input to the device. So that control devices receive correct gate voltage even after the capacitive load has been charged and the device remains inverted. To overcome some minor defects like short circuit paths or leakage mechanisms high degree of tolerance were used in the non clocked logic method .

Differential Cascode Voltage Switch (DCVS) has more advantages on the static CMOS in terms of circuit delay, layout area and power wastage. There are a more no. of DCVS variations in the basic concept which uses the pairs of differential logic inputs to flip-flop a cross coupled device pair and store an output state:

I. Differential Cascode Voltage Switch Logic (DCVSL)
II. Differential Split-Level Logic (DSL)
III. Cascode Non-Threshold Logic (CNTL)

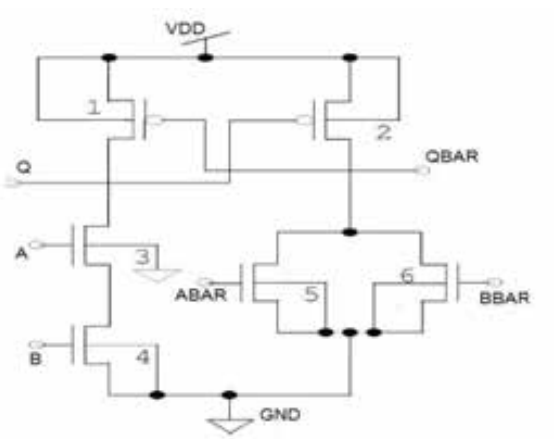

Figure5:AND Logic using DCVSL

7. DSL (Differential Split-Level logic):
DSL is an one of the technique in non clocked logic method which allows to decrease the drain-source voltage. DSL logic circuit is fully different from DCVSL. DCVSL consist of two extra NMOS transistors placed between the PMOS part. Gates are controlled by the reference voltage, the reference voltage should be equal to half of supply voltage V_{dd} + Threshold voltage of the NMOS transistors to give the optimum circuit operation.

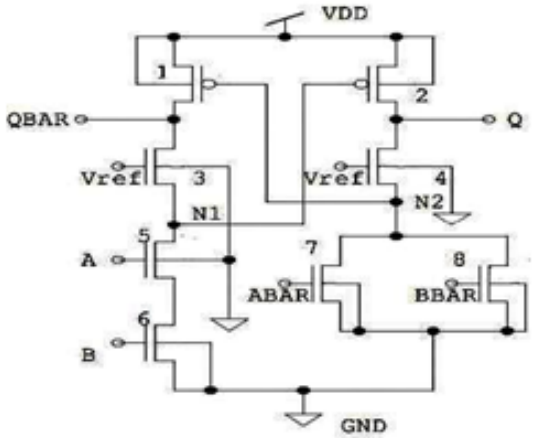

Figure6: AND Logic using DSL

Differential Split-Level logic provides quick transitions because the NMOS transister pull down device never uses drain voltage higher than , the channel hot-electron. The resistance of the reference device will reduces the height of the tree .

TABLE-2
CHARACTERISTICS OF DSL

STRENGTH	WEAKNESS
Low A.C power	Higher standby current and wasteage of power is high
Superior static performance	Requires reference voltage
High reliability	Device count is more
Chennel hot electron wearout is was reduced	
Load drive capasity is more	Substantial area increase
Immune to differential noise	Shunting capacitors are needed

TABLE-3
RESULTS FOR GATED AND NON-GATED

	Without-clockgating	With-clockgating
Area	165084	144180
Cells	938	691
Dynamic power	124677271.350(nW)	109151600.949 (nW)
Total power	124677325.047(nW)	109151648.992(nW)
Timing slack	-890ps	-896ps
Rise skew	28.6(ps)	185.2(ps)
Fall skew	28.6(ps)	150.7(ps)

Volume : 5 | Issue : 2 | Feb 2015 | ISSN - 2249-555X

8. CONCLUSIONS :

In this paper we have compared the clocked logic gate style and non clocked logic gate style from the above we can observe that non clocked logic gate style has very faster transmission speed but we can see some wasteage of power .In clocked logic style we can design a ciricuit with thousands of transister and area of the circuit is decreased .

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