RESEARCH PAPER | Engineering | Volume : 5 | Issue : 6 | June 2015 | ISSN - 2249-555X

Improving the Reliabiltiy of a SOC by Test Hole Reduction Methodologies

KEYWORDS

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ABSTRACT *Manufacturing defects can be minimized but cannot be avoided during manufacturing process. Commonly found manufacturing defects are open interconnect on the die due to dust particles; short-circuited source or drain on the transistor due to metal spike-through etc.Testability measures how easy it is to create a program to test a manufactured design's quality. Two types of tests for silicon devices are functional test and structural test. Functional testing ensures that functionality device is proper. Structural test makes sure that all transistors are present, connected correctly, and are operating as expected. Design for Testability (DFT) on-die is necessary to meet the above mentioned features. The areas which cannot be tested by structural testing in a pre-silicon environment are called 'Test holes', which requires functional test cases to ensure the logic inside the test holes are defect free. Lesser the pre silicon test holeslower the testing cost of aSoC and easier the post silicon testing process. The structural testing, which avoids the tedious functional testing is given more importance in most. In this paper, different methodologies to reduce the test holes using structural design are attempted. This methods helps to improve the time to market by cutting down on functional validation on each of the die, to meet the desired DPM(defect per million).*

Introduction:
SoC is a silicon system with different modules or Intellectual Properties (IPs) present on a single platform. Low cost, small sizeand low power consumption makes the device compact, efficient and portable. The probability that a manufacturing defect in the IC will result in a faulty chip increases with the reduction in feature size. When the feature size is less than 100 nm,very small defect can easily result in a faulty transistor or interconnecting wire. Manufacturing defect is one of the major threats that a silicon industry can face. To find out the manufacturing defects, proper test procedure should be adapted.

One of the most expensive, time consuming, and difficult things a company can do is testing its own products. Testing does not make a product more useful, prettier or easier to use.In fact it costs money. Testing is the last step in any manufacturing process; it will hold up production and slowdown or stop the shipment of revenue-producing products. Testers and the test facilities that house them cost a lot of money;thereforeevery industry wants to test their products as efficiently as possible. Wasting time in running tests, whichrepeat the test flow or seldom find anything wrong definitelyincreases the expenditure. Hence framing a test which is time and cost effectiveis essential. Testing the device minimum number of times should still guarantee the quality needed. It is better to generate the pattern before fabricationto detect the error rather than generating the same after fabricationfor an economical reason.

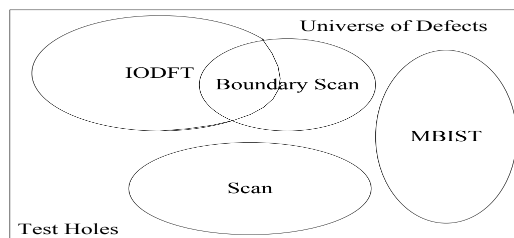

Figure 1 Venn diagram representation of test coverage and test hole.

Quality of the implemented DFT logicimpacts the design with high fault coverage. The most practical designs suffer from a variety of DFT-related issues like clock and rest controllability issue, which if left unresolved results in reduced test coverage. Thus to improve the test coverage, efficient DFT methodologies need to be adapted and an alternate plan to deplete the uncovered region is required.

Scan is a structured DFT methodology which increases the controllability and observability of a design. It connects the sequential elements (flip-flops) of a design into one or more shift registers called scan chains. These chains make a data state to be shifted into the design as well as allow the current data state to be observed by shifting out the data. Scan achieves a very high fault coverage using automated combinational ATPGalgorithms on the scanned logic using a commercial ATPG tool.

Complete chip cannot be testedeven-though many DFT methodologies like Scan, IODFT (Input Output DFT), MBIST (Memory Built In SelfTest), Boundary Scan etc… exist s. This non testability of SoC can be represented as shown in Figure 1. Test hole is an area which is not covered by above mentioned methodologies. In a chip, this should be as minimal as possible. Traditional method adapts functional verification after fabrication.Functional verification includes giving all possible inputs to the system and verifying its corresponding outputs. For 'n' input logic gate, 2^n possible inputs need to be provided. For logic with thousands of gates, it is very tedious and time consuming process to provide all the possible inputs. Observing a defect afterfabrication requires a system to modify the detected bug and retest the same. This increases the cost of manufacturingand production life cycle also. If certain methodologies to generate the test patterns to cover the test hole much before fabrication, then it becomes an alternative solution to other production life cycle reducing techniques. These patterns can be directly applied during post silicon testing, which reduces the testing time. In this paper, an attempt to reduce the test hole using different methodologies is made.This may be achieved either by-

covering untested part or by increasing area of individual circle or in Figure 1.

Design Flow:

Test coverage is a measure of the number of faults which test process can detect divided by the total number of testable faults in the device. High test coveragepoints to lower defect level. Therefore test coverage is of the highest concern as it gives the most realistic assessment of the ability to validate the correctness or error freeness of manufacturing process of the design. Fault coverage is the percentage of all faults (includes both testable and untestable) that are detected by the test patterns. The significant difference between the test coverage and fault coverage implies the design may have a lot of redundancy or tied logic or possibly even a disconnected block of logic in the netlist. The ATPG tools are much more efficient inpre-assessing combinational circuits than for sequential circuits. Hence the primary DFT approach is commonly used to implement full scan on the design.

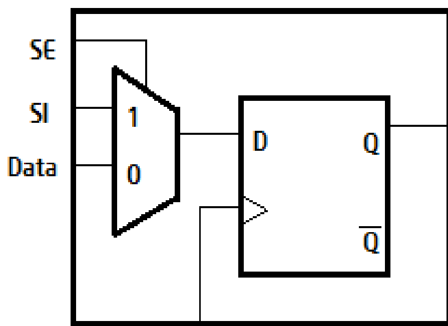

Figure 2. Scan Flop

Ana KeimWu,YangRuifengGuo and Wu-Tung Cheng presented the theoretical knowledge of scan based debug flow followed in most of the industries. F. Hapke and J. Schloeffel have used defect-Oriented Cell-Aware Test Methodology for significant reduction of DPM rates. Here test holes were found out after the synthesis. SpyGlass tool can be used to detect the test holes much before synthesis process.The practical implementation of the scan methodology and its debug flow is described in the current paper.R. Wampler compares the pre silicon coverage value with the post silicon coverage value. Lesser the test holes in pre-Si environment greater the post silicon coverage value, which is the ultimate goal of every Si industry.

Key objectives of a scan design are:

a) to allow any internal state necessary for testing to be achieved by forming shift registers called scan chains
b) to force latch enables to be active so that the latch may be treated as a buffer
c) to allow easy control of clocks so test results at internal nodes can be captured.

Flip flops are replaced by scan flops. Typical scan flop is shown in Figure 2. A critical aspect of this shifting action is that shift clocks must reach the scan flip-flops and the sets and resets must remain inactive regardless of circuit state i.e.free running clock should reach the flops and all the resets must be controllable in scan mode. Select line of the multiplexer in scan flop indicates whether circuit is in scan mode or functional mode. When select line is 1, scan in data is fed to the flip flop else the functional data will be fed to the flip flop. These scan flops are cascaded to form the scan chain. For scan stitching, clock-mixing in scan chains will be allowed, with lock-up latches inserted between clock domains in the scan chains. Some SoC products prefer to use lockup flops instead of lockup latches to help mitigate hold issues. In the case of chains having negative and positive edge flops, the negative edge flops will be placed at the beginning of the chain (close to the scan input) followed by the positive edge flops. This helps to meet timing during scan-shift.

ATPG Vector, are typicallyused to shift tests into a circuit and to capture test data using these chains.Scan Flip-flop,must be switched back to 0 so that test results can be captured for scanout.The capture clock must be operated in system mode and therefore the circuit must be designed to guarantee that the capture pulses reach thescan flip-flops regardless of the scan-in state.

The device is placed into the scan testmode using scan_ modesignal. The functional mode or mission mode of the device is by default enabled.

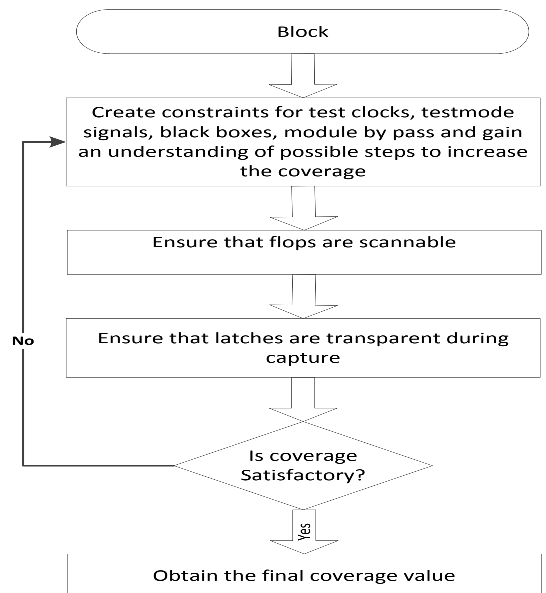

Figure 3. General Scan Flow.

Whenever scan_mode signal is 1, device works in scan mode else it works in functional mode. Thus these two modes are mutually exclusive. Some basic guidelines for scan friendly designs are

- Flops identified for scan have completely controllable clocks and resets. The clocks and resets are controllable from pins on the device interface or through JTAG/ TAP port.
- Flops that configure PLLs and clock dividers are not scannable
- Flops that are in secured mode are kept out of scan chain.
- Flops used in power-down and reset control mechanisms are non-scannable UNLESS bypassed by a signal from the pin interface, for controllability in scanmode.
- It is desirable to have each clock domain tested at-speed during transition fault testing.

Results:

SpyGlass is the predictive Analysis platform gives a powerful guidance dashboard that enables efficient verification and optimization of SoC designs early, before expensive and time-con-

Volume : 5 | Issue : 6 | June 2015 | ISSN - 2249-555X

suming traditional EDA (Electronic Design Automation) tools are deployed.DFT Compiler (DC) is another tool by Synopsis, which delivers scan DFT synthesis flows within fastest time to results. It correlates standard scan synthesis and shortens the design cycle. Both the tools increase the productivity by accounting for testability early in the design flow.

SpyGlassand DC toolsare used to find the test hole in pre silicon environment. Lesser the coverage, greater the test holes. Coverage value will be improved if the design is made scan ready. General steps to be implemented to make the design scan ready are as follows,

1. All flip-flops are scannable (unless forced/inferred "noscan")

1. All latches are transparent (unless retiming)

To make the design scan ready we may have to insert multiplexers in the design, which makes scan data to propagate instead of functional (Figure 2). All the uncontrollable resets are made controllable during scan mode. This is to make sure that every flop is a part of scan chain. Corresponding changes should be done in correspondingRTL. Once the RTL changes are done, check for the scope for optimization. If it is possible to optimize the added design, then those optimization steps are carried out. After we get the output for modified input files, coverage values are compared. Figure 3. shows the general scan flow.

```
   Base stuck-at fault coverage :98.6
   Base stuck-at test  coverage :98.6

lote: Coverage reported may be over-optimistic due to test_mode defined on internal nodes.
     Please refer to Scan_07 messages for more details on test_mode specified on
     internal design nodes.

   Expected stuck-at coverage data after each step.
                                 Expected stuck-at coverage
                              ---------------------------------
                                     FC        TC              Action
 ---------------------------------------------------------------------------------------
   0. Original Design                98.6      98.6      No DFT changes are made.It assumes
                                                         'scan' declared flip-flops scannable.
                                                         Use Info_forcedScan to detect such
                                                         flip-flops
   1. Flip-flops made scannable      98.6      98.6      No action required
   2. Scan-wrap black boxes          98.6      98.6      No action required
   3. Latches made Transparent       98.6      98.6      No action required
   4. Combinational Loops made
      controllable                   98.6      98.6      No action required
   5. Testmode/Tied pins made
      controllable                   99.9      99.9      Info_synthRedundent, Info_untestable
                                                         and Info_pwrGndSim.
                                                         Add -scanshift switch to test_mode
                                                         constraint, if appropriate
   6. Hanging nets made controllable 99.9      99.9      TA_09
   7. Tristate enables made observable 99.9    99.9      No action required
   8. 'force_ta' and 'test_point'
      constraint pins made testable  99.9      99.9      No action required
   9. 'no_scan' flip-flops made
      scannable                      100.0     100.0     Use Info_noScan & Info_inferredNoScan
                                                         to view all no_scan flip-flops
```

Figure 4.SpyGlass Report showing the stuck at coverage value after test hole reduction for block 1.

Different goals can be run to check the scan ability of the device in SpyGlass. These goals include dft_setup, dft_stuck_at_coverage, dft_scan_ready, dft_latches etc. Most of the required results are obtained by running dft_scan_ready goal. It gives the violations for the non scanable part. One needs to trace back the signals and find out the reason for non scanability. Schematic diagram can be used to trace the signals. If RTL changes are required, then corresponding changes are performed to achieve higher coverage value. Regression testing is carried out on the modified RTL.

Figure 4 shows the report generated by SpyGlass after running stuck at fault coverage goal. Base stuck at coverage field in the report gives the current design coverage for the given RTL input. It also gives the steps to improve that coverage value. In most of the cases, rectifying the reported violations will increase the coverage. Figure 4 is the report generated for one block of a Soc. Schematic diagramis mostly used to trace the signals. Ultimate goal is to bring the coverage value to more than 95% by making corresponding RTL. Required additional design is incorporated to ease the post silicon

```
           Pattern Summary Report
 -----------------------------------------------
 #internal patterns                           0
 -----------------------------------------------


     Uncollapsed Stuck Fault Summary Report
 -----------------------------------------------
 fault class                     code   #faults
 ------------------------------  ----  ---------
 Detected                         DT    4365486
 Possibly detected                PT      20462
 Undetectable                     UD      534[illegible]0
 ATPG untestable                  AU     765783
 Not detected                     ND      35917
 -----------------------------------------------
 total faults                           5241078
 test coverage                           84.35%
 -----------------------------------------------
  Information: The test coverage above may be inferior
               than the real test coverage with customized
               protocol and test simulation library.
```

Figure 5. DC Report showing the stuck at coverage value after test hole reduction for block 1.

testing. Figure 5 shows the DC report. DC will give more accurate coverage value than SpyGlass. But this can only be run after the RTL synthesis.Hence before the synthesis process, we can use spyglass and filter out the major issues.

Conclusion:

Scan being structural testing detects the controllability and observability issues. Detection of test holes in early stage of a SoC is needed. Performing scan test on RTL is one of the efficient methods to do that. This will reduce the test holes (by increasing the area of circle in figure 1) in actual Si and corresponding functional tests can be avoided. This reduces the cost of testing, which every industry aims at. Meanwhile care is taken that DPM value is not effected with this structural testing method.

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