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Additive Noise Response of Some Novel Phase Detector Based Charge Pump PLL Circuits; an Analytical and Simulation Study

KEYWORDS: tracking performance, mean square tracking error, mean square loop oscillator phase jitter

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ABSTRACT *An analytical and simulation study of a new phase detector based charge pump PLL circuit in the field of a noisy input signal has been reported here. A comparison of the said study with Hogge phase detector based charge pump PLL circuit is also reported here. Finally merit of the new phase detector based charge pump PLL circuit has been established by some extensive simulation results.*

INTRODUCTION

In literature, the analytical and experimental performance of a new phase detector (NPD) based CDR circuit with noise free input signal had been reported [1]. However, in reality at the time of transmission of the signal through the channel or medium, it has been suffered from several noises coming from channel or medium. So to realize the practical applicability of the NPD based CP-PLL system it is very important to measure the tracking performance of the circuit with noisy input signal and then comparing with the results found from CP-PLL circuit with Hogge phase detector (HPD) [2], the merit of the NPD based CDR circuit may be established in the field of noisy input signal. The tracking performance measures, the amount of phase error between two input signals of the phase detector (PD) that can track by the loop when the loop is under locked condition or in another way we have to measure the tracking performance (i.e. mean square tracking error and mean square loop oscillator phase jitter) of CP-PLL circuit when a noisy signal is applied at the input of PD under locked condition.

In case of charge pump PLL (CP-PLL) using NPD, the amplitude of the input signal would be limited and the angle part of the signal would be actual concern. So, in the case of CP-PLL system the presence of additive noise with the input signal can be taken into account by adding a random phase component (taking as $\psi(t)$) with the input signal phase [3, 4]. It will result in random fluctuation of zero crossing sampling instants of the input signal. As such the phase tracking error detected by the loop NPD will fluctuate randomly.

ANALYTICAL ESTIMATION OF TRACKING PERFORMANCE FOR CP-PLL STRUCTURE WITH NPD IN THE FACE OF NOISY INPUT SIGNAL

Fig.1a shows a CP-PLL taking loop phase detector (PD) as NPD and Fig.1b shows hardware circuit diagram of NPD. The mean square (MS) values of phase tracking error determined the tracking performance of the CP-PLL system with NPD. The tracking error (θ_e) can be defined as the difference of input signal phase (for this system noisy input signal) and the loop oscillator (LO) phase.

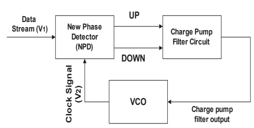

Fig.1.a Block diagram of the PLL based CDR circuit using new phase detector.

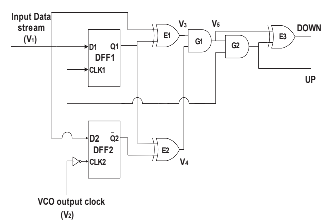

Fig.1.b Hardware structure of a new phase detector comprises with two D-flip/flops (DFF), three EX-OR gates and two AND gates.

However one can define the LO output phase jitter, denoted by ξ as the displacement of LO phase related to and input signal phase free from all jitters. Minimum of these quantities indicates better performance. Since the steady state phase error for NPD based CP-PLL system is zero [1] and at that time VCO control voltage does not contain any fluctuations, so for analytical prediction one can consider the phase value only at input data transitions.

It is obvious that for the Charge Pump PLL (CP-PLL) structure with NPD, if there is a phase error of amount (θ_e) between an input signal of frequency (ω_i) and VCO output signal of frequency (ω_0) one can gets an effective pump ON interval of approximate duration $\theta_e/\omega_i(=t_p)$ at each transition instants of the input data stream. If I_P be the pump current magnitude then VCO control voltage is obtained by passing the pump current through the filter impedance function comprised of resistor R and capacitor C of time constant τ (= RC

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). According to the analysis of Gardner [5] the different system parameters for the loop is given below.

$$K = \frac{K_0 I_P R}{2\pi},\ \omega_n = \sqrt{\frac{K}{\tau}},\ \rho_0 = \frac{\omega_n \tau}{2},\ C_1 = \frac{2\pi K}{\omega_i}$$

Where K_0, K, ω_n, ρ_0 and C_1 are called loop VCO sensitivity, loop gain or loop bandwidth, loop natural frequency loop damping factor and normalized loop bandwidth respectively. Assuming input signal phase error and VCO phase at time t as $\theta_i(t)$ and $\theta_0(t)$ respectively and choosing the time origin at the active transition instant of input signal, $\theta_i(t)$ and $\theta_0(t)$ can be written in the first cycle (until the next UP or DOWN pump current starts) as

$$\theta_i(t) = \theta_i(0) + \omega_i t \qquad (1)$$

When input data stream lead the regenerated clock signal then VCO output phase can be written as (for details see Appendix-A)

$$\theta_0(t) = \theta_0(0) + \omega_0 t + K_0\left[V_x(0)t + i_P R t + \frac{i_P}{2C}t^2\right]$$

for $0 < t < t_p$ (2)

$$\theta_0(t) = \theta_0(0) + \omega_0 t + K_0\left[V_x(0)t + i_p R t_P - \frac{i_p t_P^2}{2C} + \frac{i_p t_P t}{C}\right]$$

for $t_p < t < T_i$ (3)

where $T_i = \frac{2\pi}{\omega_i}$ is the input signal time period and

$i_p = I_P\, Sgn(\theta_e)$.

If $\theta_e(t) = \theta_i(t) - \theta_0(t)$ is represent the phase error at any time t then we can write

$$\theta_e(t) = \theta_e(0) + (\Delta\omega - K_0 V_x(0))t - K_0\left[i_p R t + \frac{i_p t^2}{2C}\right]$$

for $0 < t < t_p$ (4)

$$\theta_e(t) = \theta_e(0) + (\Delta\omega - K_0 V_c(0))t - K_0\left[i_p R t_P - \frac{i_p t_P^2}{2C} + \frac{i_p t_P t}{C}\right]$$

for $t_p < t < T_i$ (5)

where $\theta_e(0)$ is the initial phase error, $\Delta\omega = \omega_i - \omega_0$ and $i_p = I_P \operatorname{sgn}(\theta_e)$ or $i_p t_p = I_P \frac{\theta_e(t)}{\omega_i}$

From above equation we can find the steady state phase error (θ_{es}) and steady state VCO control voltage (V_{xs}) as (see Appendix-A),

$\theta_{es} = 0$ and $V_{xs} = \Delta\omega / K_0$

So considering this we can write mathematically the expression for tracking error using eqn's (4) and (5) as follows.

$$\theta_e(n) = \theta_e(n-1) + \left(\Delta\omega - K_0 \frac{i_p}{C}\sum_{j=1}^{n-1}\frac{\theta_e(n-j)}{\omega_i}\right)T_i - K_0\left[i_p R - \frac{i_p}{2C}\frac{\theta_e(n-1)}{\omega_i} + \frac{i_p}{C}T_i\right]\frac{\theta_e(n-1)}{\omega_i} + \psi(n)$$

(6)

or

$$\theta_e(n) = \theta_e(n-1) + \sum_{j=1}^{n}\psi(j) - \sum_{j=1}^{n}\zeta(j) \qquad (7)$$

To examine the tracking response of the loop, one can write the discrete difference equation of the loop phase error in the face of noisy input signal for NPD based CP-PLL system with the help of equation (6) as, neglecting the higher terms involving θ_e [3]

$$\theta_e(n+1) = a\theta_e(n) + b\theta_e(n-1) + \psi(n+1) - \psi(n) \qquad (8)$$

where $a = (2 - r_1 C_1)$, $b = (C_1 - 1)$ and r_1, C_1 stand for $\left(1 + \frac{2\pi}{\omega_i \tau}\right)$ and $\left(\frac{2\pi K}{\omega_i}\right)$ respectively. Now the jitter of LO output at n-th active transition instant can be determined from eqn (7) as

$$\zeta(n) = \theta_e(n-1) - \theta_e(n) + \psi(n) \qquad (9)$$

It is found that the sample values of $\psi(t)$ are statistically independent from one another and because of obvious reasons, $\psi(t)$ sample value of present instant is independent of θ_e samples of previous instants and hence remembering these, one can write:

$$\overline{\psi(i)\psi(j)} = \overline{\psi^2}\delta_{ij} \qquad (10a)$$

$$\overline{\theta_e(n)\psi(m)} = 0 \qquad (10b)$$

Here the notation "overbar" is used to denote the statistical averaging process, δ_{ij} is the Kroneker delta function. Also in equation (10b) m-th instant is considered after the n-th instant and so the input perturbation $\psi(m)$ will have no correlation with the

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tracking error $\theta_e(n)$ of some previous instant. Considering $\psi(t)$ as a zero-mean process, the mean values of θ_e and ζ are obtained as zero from (8) and (9). The MS value of tracking error $\overline{\theta_e^2}$ can be obtained from (8) using (10a) and (10b). The simplified expression for the same can be obtained as [3]

$$\overline{\theta_e^{\,2}} = \frac{2\overline{\psi^2}}{\left((1+b)(1+a-b)\right)} \tag{11}$$

In a similar way, the MS value of the LO output jitter $(\overline{\zeta^2})$ can be obtained from (9) using (10) and (11) as follows:

$$\overline{\zeta^2} = \frac{2}{(1-b)}\left[(1-b-a)\overline{\theta_e^{\,2}} + \left(\frac{1+b}{2}\right)\overline{\psi^2}\right] \tag{12}$$

Since $\overline{\theta_e^2}$ and $\overline{\psi^2}$ both have positive finite values one can finds from (11) that b should be less than $(1+a)$ or $C_1 < \frac{4}{(r_1+1)}$. This can be used to find the stability condition of the system. Again, since the minimum value of r_1 can be 1 (when $\omega_i\tau \to \infty$) the maximum value of C_1 would be 2 and that can also be seen from (12).

Now considering the randomness of the input phase $\psi(t)$ is due to presence of a band limited Gaussian noise *n(t)* with the desired input signal of the loop, the probability density function (pdf) $(P(\psi))$ of $\psi(t)$ can be written as [6]

$$) = \left(\exp(-\rho) + \sqrt{\pi\rho}\cos\psi\exp\left(-\rho\sin^2\psi\right)\right)\left(1 + erf\left(\sqrt{\rho}\cos\psi\right)\right)) \tag{13}$$

Where $erf(x)$ is the error function of argument x and ρ is the input signal to noise power ratio (SNR). ρ can be determined from the variance (σ^2) of random phase noise as, $\rho = 1/(2\sigma^2)$ [6]. Using this "pdf" one can find the MS value of the input random phase, $\overline{\psi^2}$ in terms of the signal to noise power ratio (SNR), ρ as

$$\overline{\psi^2} = \frac{1}{2\pi}\int_{-\pi}^{\pi}\psi^2 P(\psi)\, d\psi \tag{14}$$

or,

$$\overline{\psi^2} = \frac{1}{2\pi}\int_{-\pi}^{\pi}\overline{\psi^2}[\exp(-\rho) + \sqrt{\pi\rho}\cos\psi\exp(-\rho\sin^2\psi).(1 + erf(\sqrt{\rho}\cos\psi))]d\psi \tag{15}$$

ANALYTICAL AND SIMULATION STUDIES

For a given SNR the MS values of tracking error and MS values LO output jitter for CP-PLL system with HPD and NPD, obtained from (11) and (12) using (15) are plotted in the Fig. 9 and Fig. 10 as a function of normalized loop bandwidth (C_1) and normalized loop natural frequency. Again for a given normalized loop bandwidth (C_1) and normalized loop natural frequency $(2\pi\omega_n/\omega_i)^2$ the MS tracking error and MS LO Phase jitter are plotted in Fig.11a and Fig.11b respectively as a function of inverse SNR (ρ^{-1}). Since in CP-PLL system the pump on interval for equal magnitudes of negative and positive phase tracking errors are unequal, the expression should be written by considering mean pump ON interval. For positive and negative values of phase error $\theta_e(n-1)$, $t_p(n)$ can be expressed [3,6] as

$$t_{p\pm}(n) = \frac{2|\theta_e(n-1)|}{\omega_i[1-\operatorname{sgn}\theta_e(n-1)] + \omega_0(n)[1+\operatorname{sgn}\theta_e(n-1)]} \tag{16}$$

Where $\omega_0(n)$ is the average frequency (rad/sec) of VCO during $t_{p+}(n)$. $\omega_0(n)$ can be obtained from the following relation

$$\omega_0(n) = \left(t_{p+}(n)\right)^{-1}\int_0^{t_{p+}(n)}\omega_i\left[1 + C_1\sum_{l}^{n-1}\frac{t_{p+}(l)}{\tau} + C_1\left(1 + \frac{K}{\omega_i\tau}\right)\right]dx \tag{17}$$

For small tracking error the summation term and the term containing $t_{p+}(n)$ can be neglected and then the pump ON interval can be expressed as

$$t_{p\pm}(n) = \frac{|\theta_e(n-1)|}{\omega_i\left[1 + \frac{C_1}{2}\left(1+\operatorname{sgn}\theta_e(n-1)\right)\right]} \tag{18}$$

Now using this equation (18) in equation one can obtain the mean pump ON interval as

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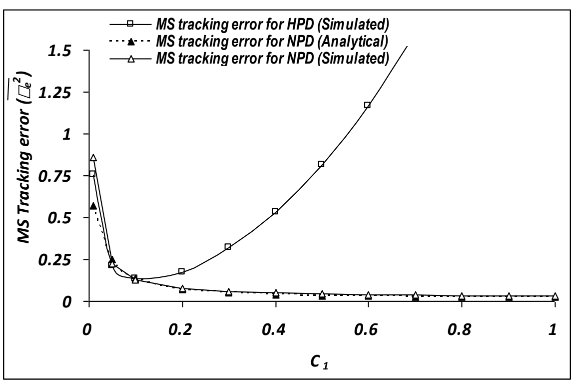
$$t_p(n) = \frac{\theta_e(n-1)}{\omega_i}\left[\frac{\left(1+\frac{C_1}{2}\right)}{(1+C_1)}\right] \quad (19)$$

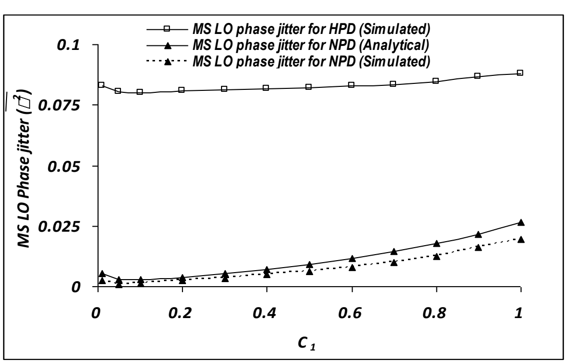
From this equation one can write the mean pump ON interval in terms of C_{11} instead of C_1 where

$$C_{11} = \frac{C_1\left(1+\frac{C_1}{2}\right)}{1+C_1} \quad (20)$$

The analytical values of $\overline{\theta_e^{\,2}}$ and $\overline{\psi^2}$ are verified by comparing them with the computer simulation results. To carry out the computer simulation, a large set of random $\psi(t)$ samples is generated from a large set of Gaussian samples of prefixed mean and variance. Taking a sample of this set as a random component of the input signal phase at a particular data transition instant, we find the values of phase error at each active data transition instant of the loop NPD. These sample values are used to obtain the MS values of tracking error and MS values of LO phase jitter. The simulation results as well as analytical results have been shown in Fig.9, Fig.10 and Fig.11 for HPD and NPD based CP-PLL. These results indicates that the tracking performance is improved and LO phase jitter is reduced for the NPD based CP-PLL structure.

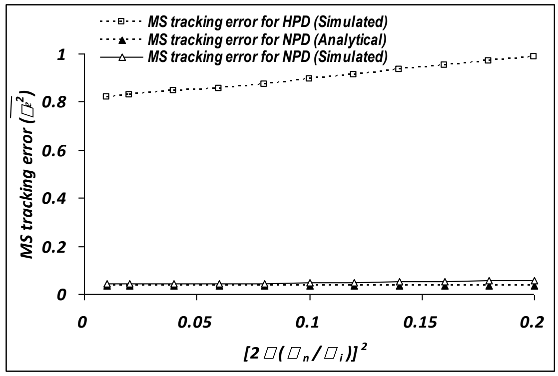


(a)

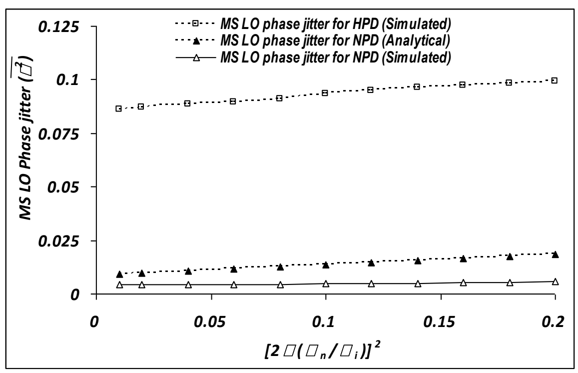


(b)

Fig. 9 Variation of (a) MS values of tracking error in rad² and (b) MS values of LO phase jitter in rad² with normalized loop bandwidth (C_1); taking $\rho = 20$, $(2\pi\omega_n/\omega_i)^2 = 0.01$, for both HPD and NPD based CP-PLL system.

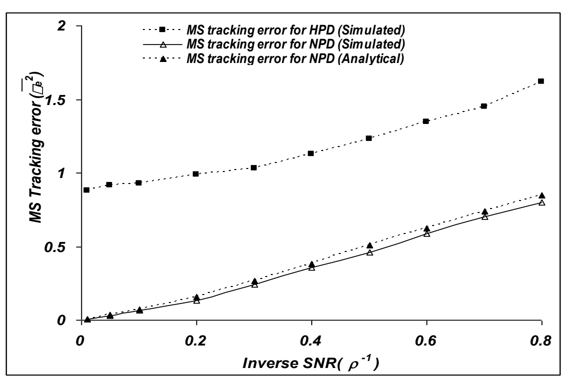


(a)



(b)

Fig. 10 Variation of (a) MS values of tracking error in rad² and (b) MS values of LO phase jitter in rad² with normalized loop natural frequency $\left((2\pi\omega_n/\omega_i)^2\right)$; taking $\rho = 20,\ C_1 = 0.5$, for both HPD and NPD based CP-PLL system.



(a)

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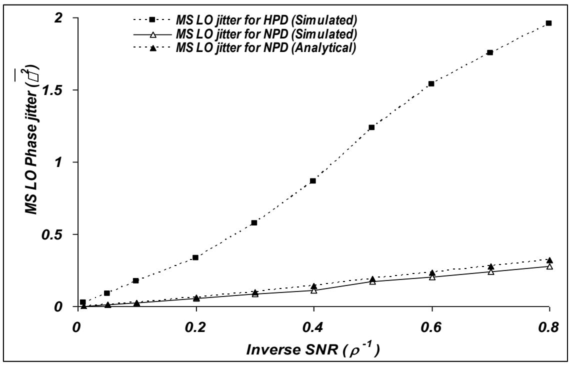

(b)

Fig. 11 Variation of (a) MS tracking error in rad^2 and (b) MS LO Phase jitter in rad^2 with inverse SNR (ρ^{-1}) for HPD based and NPD based CP-PLL system; taking $(2\pi\omega_n/\omega_i)^2 = 0.01$ and $C_1 = 0.5$

CONCLUSIONS

The tracking performance of the proposed modified system in the face of noisy input signal is also examined by analytical means and by simulation studies. It has been found that the proposed system has better tracking performance than the conventional system. So the proposed NPD based CDR circuit has some merits in view of tracking response when noisy

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APPENDIX-A

MATHEMATICAL MODELLING OF CP-PLL USING NEW PHASE DETECTOR (NPD)

In a NPD a pair (such as UP and DOWN) of digital pulses has been generated depending upon the corresponding phase error between the input signal and VCO output signal. Here the pulse width of UP/DOWN output terminals of the NPD can very within the range of VCO clock period depending upon the amount of phase error. When input signal leads or lags the VCO signal then UP or DOWN terminal contains a pulse with width proportional to phase error. The charge pump circuit then converts the digital pulses into an analog current that is converted to a voltage via the passive loop filter network. The resulting control voltage drives the VCO. If the pump current ON interval is denoted by t_P, then for small phase error (θ_e), one can approximate t_P as,

$$t_P = \frac{|\theta_e|}{\omega_i} \qquad \text{(A.1)}$$

where ω_i is the input signal angular frequency in rad/sec.

Now if $\theta_i(t)$ and $\theta_0(t)$ are the input signal phase and output signal phase at any time, t then one can write the expression for them in real time as,

$$\theta_i(t) = \theta_i(0) + \omega_i t \qquad \text{(A.2)}$$

$$\theta_0(t) = \theta_0(0) + \omega_0 t + K_0 \int_0^t V_c(\tau)\,d\tau \qquad \text{(A.3)}$$

where

$$V_c(t) = i_P R + V_x(t) \qquad \text{(A.4)}$$

$$V_x(t) = V_x(0) + \frac{1}{C}\int_0^t i_P(\tau)\,d\tau \qquad \text{(A.5)}$$

$$i_P = I_P \operatorname{sgn}(\theta_e) \quad \text{for } 0 < t < t_P \qquad \text{(A.6a)}$$

$$i_P = 0 \quad \text{for } t_P < t < T_i \qquad \text{(A.6b)}$$

and ω_0 is the angular frequency of VCO output signal, K_0 is the VCO sensitivity in rad/sec/volt. And R & C are the loop filter resistance and capacitor respectively

Now using (A.4), (A.5) and (A.6) in (A.3) one can write

$$\theta_0(t) = \theta_0(0) + \omega_0 t + K_0\left[V_x(0)t + i_P R t + \frac{i_P}{2C}t^2\right]$$

$$\text{for } 0 < t < t_P \qquad \text{(A.7a)}$$

and

$$\theta_0(t) = \theta_0(0) + \omega_0 t + K_0\left[V_x(0)t + i_p R t_P - \frac{i_p t_P^{\,2}}{2C} + \frac{i_p t_P t}{C}\right]$$

$$\text{for } t_P < t < T_i \qquad \text{(A.7b)}$$

So the phase error (θ_e) can be written as,

$$\theta_e(t) = \theta_i(t) - \theta_0(t)$$

or,

$$\theta_e(t) = \theta_e(0) + (\Delta\omega - K_0 V_x(0))t - K_0\left[i_p R t + \frac{i_p t^2}{2C}\right]$$

$$\text{for } 0 < t < t_P \qquad \text{(A.8a)}$$

and

$$\theta_e(t) = \theta_e(0) + (\Delta\omega - K_0 V_x(0))t - K_0\left[i_p R t_P - \frac{i_p t_P^{\,2}}{2C} + \frac{i_p t_P t}{C}\right]$$

$$\text{for } t_P < t < T_i \qquad \text{(A.8b)}$$

where $\Delta\omega = \omega_i - \omega_0$ and $\theta_e(0) = \theta_i(0) - \theta_0(0)$

Steady state phase error (θ_{es}) for NPD based CDR circuit can be written using the conditions (i) $t_p = 0$ and (ii) $\Delta\omega - K_0 V_x(0) = 0$ in equation (A.8) as,

$$\theta_{es} = 0$$

And steady state VCO control voltage can be written using above condition (ii) as,

$$V_{xs} = \frac{\Delta\omega}{K_0}$$

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