



Design Of High-Speed, Low-Power Frequency Dividers For High Speed Frequency Synthesizer In 0.18 μm Cmos Process

KEYWORDS

Low power, Frequency divider, High Speed, CMOS Technology

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ABSTRACT The CMOS technologies offer the high speed and low power dissipation which is required in multi-gigahertz communication systems such as optical data links and wireless products. This paper will cover design tradeoffs in frequency divider which are maximum operating frequency, power consumption and number of transistors needed. Analog approach is adopted in design of Frequency divider. The design of communication circuits, namely a 1/2 frequency divider is fabricated using a 0.18 μm CMOS process. The divider achieves a maximum speed of ~3GHz with a power dissipation of 1mW.

INTRODUCTION

The frequency divider is an important building block in today's RFIC and microwave circuits because it is an integral part of the phase-locked loop (PLL) circuit [1]. The ever-growing popularity of CMOS devices has made them the mainstream technology for designing complex monolithic systems with dense logic, low power dissipation, low supply voltage, and highly automated synthesis. In high-speed applications, however, the relatively low transconductance of MOSFET's often compels severe speed power trade-offs, thereby limiting their advantage over silicon bipolar devices [2,3]. These trade-offs are however relaxed as device dimensions scale down, making deep submicron CMOS attractive even for multi-gigahertz circuits. This can ultimately lead to monolithic integration of communication systems that include high-speed input and output interfaces as well as extensive intermediate signal processing. This paper describes the design of two high-speed, lowpower communication circuits fabricated in a partially scaled 0.18 μm CMOS technology. The first circuit is a 1/2 frequency divider that operates with input frequencies as high as of ~1GHz with a power dissipation of 1mW. The conventional 1/2 Frequency divider is as shown in Fig. 1.

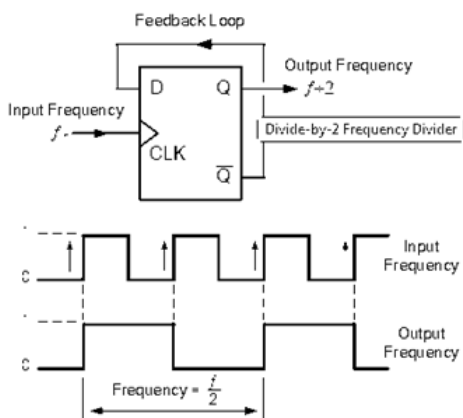


Fig. 1. The conventional 1/2 Frequency divider

Frequency divider with conventional d-flip flop

The following Fig. 2 shows schematic of Traditional D flip-flop respectively which is used to design the frequency divider.

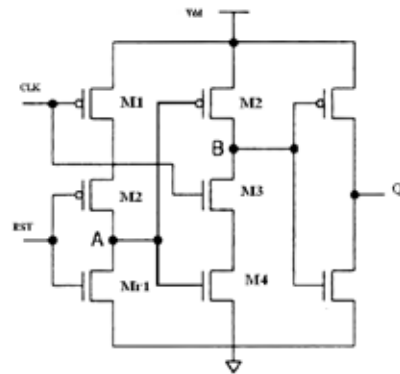


Fig 2. Schematic of Modified D flip-flop

The operations of the proposed D flip flop are very simple. When input clock and reset signals are low, the node A is connected to V_{DD} through M₁, M₂ and charges the node A to V_{DD} as shown in Fig. 2. At the rising edge of the clock signal, output node is connected to ground through M₃ and M₄. Once the node A is charged to V_{DD}, the output node is not affected by input clock signal. Because the charges at node A turn off the M₃ and this avoids the output node from pulled up. Therefore, the output node is disconnected from input node. When the reset signal is applied, node A is detached from V_{DD} by Mr₁ and connected to ground by Mr₂. As soon as the node A is discharged, the output node is pulled up through M₂. The mr1 is added to stop the short circuit that happens whenever the reset signal is applied. If the clock signal is low in the condition of reset signal is high, a current path is made from V_{DD} to ground without Mr₁. This increases the power consumption. Moreover, the reset time is increased because M₁ charges the node A to V_{DD} while the Mr₂ discharges node A to ground. Fast discharging node A means the fast reset operation.

Frequency divider with Master slave d-latch

The 1/2 frequency divider employs 2 D-latches in a master-slave configuration with negative feedback. In high speed master-slave dividers, it is common practice to design the slave as the "dual" of the master [Fig. 3(a)] so that they can be both driven by a single clock [4,5]. However, duality requires one of the latches to incorporate PMOS devices in the signal path, therefore lowering the maximum speed. To avoid this difficulty, as shown in Fig. 3(b), the divider utilizes two identical D-latches that are driven by complementary clocks CK and \overline{CK} .

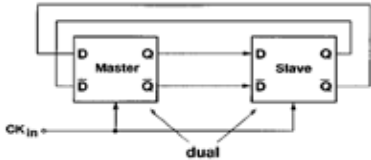


Fig 3(a) Master-slave dividers with single clock

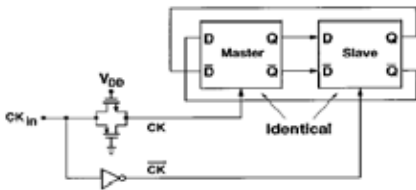


Fig. 3 (b) Master-slave dividers with complementary clocks

In order to minimize the skew between CK and \overline{CK} , the non inverted phase is delayed by means of a complementary pass gate having devices identical with those in the master. Although the skew increases as the input transition time becomes comparable with the period, simulations indicate that it is less than 5ps for a 1 GHz sinusoidal input. Fig. 4. depicts the frequency divider circuit. Each latch consists of two sense devices such as M_1 and M_2 in the master and M_7 and M_8 in the slave, a regenerative loop such as M_3 and M_4 in the master and M_9 and M_{10} in the slave, and two pull-up devices M_5 and M_6 in the master and M_{11} and M_{12} in the slave.

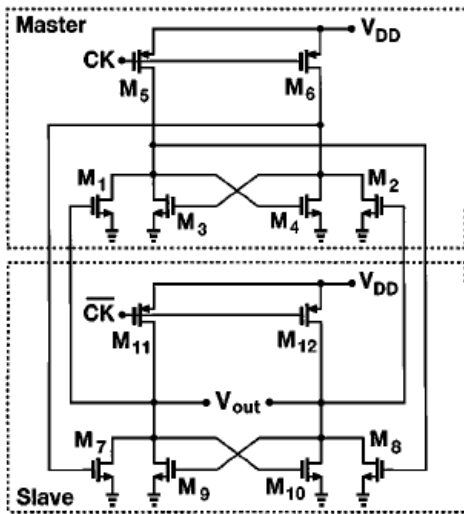


Fig.4. Frequency Divider circuit with Master Slave Flip Flop

When CK is high, M_5 and M_6 are off and the master is in the sense mode, while M_{11} and M_{12} are on and the slave is

in the store mode. When CK goes low, the reverse occurs. Note that the circuit uses no stacked or pass transistors. Also, the gate channel capacitance of the PMOS transistors hardly disturbs the critical path because these devices are (velocity) saturated almost for the entire voltage swing. At maximum speed, these swings are not rail-to-rail. In contrast with conventional latch topologies, the D-latch circuit used in this divider does not disable its input devices when it goes from the sense mode to the store mode. While this would pose timing glitches in a general digital circuit, it does not prevent the divider from functioning properly. To explain the reason, we make two observations. First, since the input devices of each latch are N-type, they can change the state only if one of the inputs goes from low to high (and the other from high to low). Second, when each latch is in the sense mode, neither of its outputs can go from low to high because the PMOS pull-up devices are off. Thus, if, for example, the master is in the sense mode and the slave in the store mode, the master's outputs can only go from high to low and hence cannot override the state stored in the slave.

Simulation result

The conventional frequency divider based on D Flip Flop is simulated on Tanner 13 in 0.18 μ m CMOS process with 1.8V supply voltage. Fig 5. shows the output waveforms of D Flip Flop and Fig. 6. shows the output wave forms of conventional 1/2 frequency divider

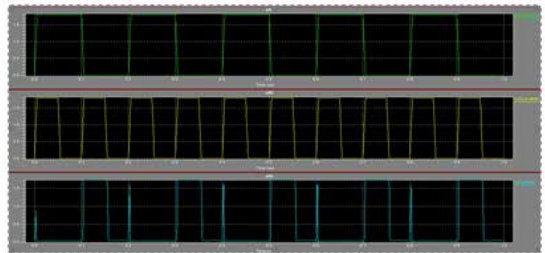


Fig 5. The wave forms of Modified D flip flop when the input CLK and RST are in phase

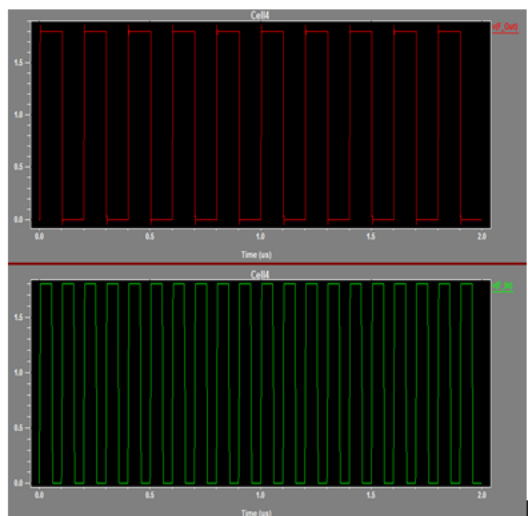


Fig 6. The output wave forms conventional 1/2 frequency divider

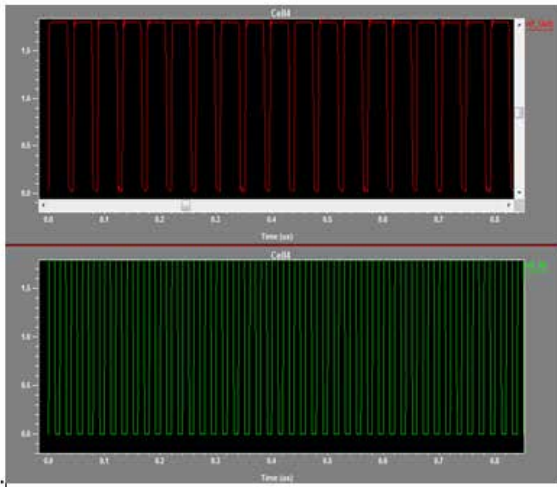


Fig 7. The output wave forms of proposed 1/2 frequency divider

The proposed frequency divider based on Master-Slave D-Latch is also simulated on Tanner 13 in 0.18μm CMOS process with 1.8V supply voltage. Fig 7. Shows the output wave forms of proposed 1/2 frequency divider. Simulation result shows that Master slave divider having good frequency response (2MHz - 2.3GHz) @ < 1mW power consumption. The performance analysis of conventional frequency divider and Master slave frequency divider shows in table 1. The layout of Frequency divider is shown in Fig. 8.

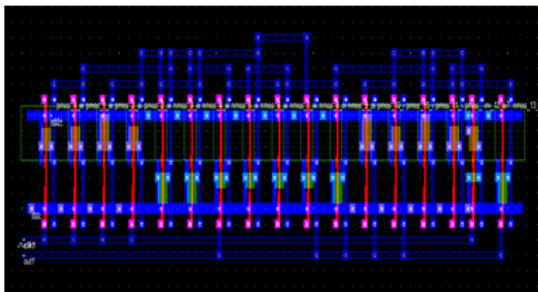


Fig. 8. Layout of Frequency Divider

TABLE 1: PERFORMANCE ANALYSIS OF CONVENTIONAL FREQUENCY DIVIDER AND MASTER SLAVE FREQUENCY DIVIDER

Parameters	Conventional Frequency Divider	Master Slave Frequency Divider
Technology	0.18μm	0.18μm
VDD	1.8V	1.8V
F _{out}	20KHz – 1.8GHz	2MHz -2.3GHz
Number of Inverters	2	Nil
Power	2.5mW	<1mW
Number of Transistor used	24 (Two D Flip Flop)	12

The post layout simulation result shows that Frequency divider using Master slave flip flop is more suitable for High frequency Synthesizer implementation. The total area consumed by frequency divider using Master slave configuration is 756.3μm² as shown in Fig. 9.

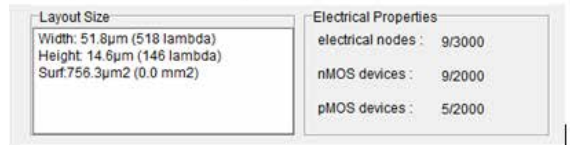


Fig. 9. Surface area required for Frequency Divider

CONCLUSION

This paper demonstrates two techniques for designing Frequency dividers using Conventional D Flip Flop and Master-Slave D=Flip Flop which is simulated with operating clock frequency greater than 1GHz. The performance analysis of conventional frequency divider and Master slave frequency divider shows that the power consumption and frequency division accuracy of Master slave divider is superior than conventional frequency divider. The Master slave divider having good frequency response (2MHz - 2.3GHz) @ < 1mW power consumption. The maximum power supply required is 1.8V. The total area consumed by frequency divider using Master slave configuration is 756.3μm².

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