Original Research Paper

Volume - 7 | Issue - 5 | May - 2017 | ISSN - 2249-555X | IF : 4.894 | IC Value : 79.96

Engineering

# Design and Implementation of High-performance Logic Arithmetic Full Adder Circuit based on FinFET Technology – Shorted Gate Mode

**Sarita Chauhan**

**Mamta kasotiya**

**Nishi chouhan**

**Sheetal Mundra**

**ShivangiAgarwal**

**ABSTRACT** Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS at the Nano scale. FinFETs are double gate and multi-gate devices. Double-gate (DG) FinFETs has better Short Channels Effects (SCEs) performance compared to the conventional CMOS and stimulates technology scaling. The two gates of a FinFET can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. In this paper, we are designing a Double-gate (DG) FinFETs and extracting their transfer characteristics by using Synopsys TANNER-EDA simulation tool. Full Adder is implemented in CMOS with technology and FinFET-shorted gate mode with technology along with its working waveform and performance analysis. TANNER-EDA simulations are carried out for the design and results are analyzed.

**KEYWORDS :** Double-gate FinFET (DG FinFET), Multi-gate (MG), Short channel effects (SCE), Shorted-Gate Mode (SG-Mode), Drain Induced Barrier Lowering (DIBL), Full Adder.

## Introduction

Since the fabrication of an MOSFET, the minimum channel length has been shrinking continuously. The primary goal of scaling of MOSFET is to achieve the speed and efficiency but it will fails in the area of leakage. The motivation behind the decrease has been a increasing interest in the high speed devices and very large scale integrated circuits. The key limitation is the short channel effect (SCE) which is caused as the length of the channel is reduced leading to the lowering of the drain potential as drain source voltage which increases allowing the flow of the electrons . This is called a Drain Induced Barrier Lowering (DIBL) .

In order to reduce these problems, FinFET is introduced which is a double gate metal oxide semiconductor field effect transistor. FinFETs offer interesting power-delay tradeoffs and better characteristics (SCE) in nanometer regime. The back gate is present, with an input voltage supply that has more controllability over conducting channel, which minimizes the short channel effect. The unique feature of the FinFET is that it has a fin shaped body perpendicular to the wafer surface which carries the current . The fin shaped body is made of ultra-thin silicon (Si). The fin acts as the conducting channel which will be controlled by the double gates and allows better controllability. The improved gate control also provides lower in the output conductance, which will also provide greater voltage gain. As the FinFET technology extends to Moore's law in all the ways, it is completely compatible with the conventional CMOS. Thus making a fabrication processes easier . Speed and area which is also important parameters and proper tradeoff between them should be drawn while designing a circuit. FinFET is well known to reduce leakage currents and hence by using FinFET technology the high leakage current problem has overcome.

Furthermore, the bulk architecture is required for a high channel doping density which is required to control the short channel effects, this leads to the large transversal electric fields and also unacceptable degradation of electron mobility. Because of the non-planar structure, the width quantization effect of the FinFET devices are still suffering from the issues, that is process complexity and the additional parasitic capacitance . Anyway it is promising candidate for the nanometer regime.

This paper is organized as follows; Section 2 explains the double-gate (DG) FinFET structure and simulation setup. The section 3 explains the different modes of operations of FinFET. The design and implementation of the cmos and FinFET full adder bridge circuits in section 4. The Section 5 describes the simulation results and discussion of cmos and FinFET logic arithmetic full adders and finally Section 6 concludes the paper.

## I. FinFET Structure:

Figure 1 shows the basic structure of a FinFET. The device is formed on the thin silicon on insulator (SOI) finger termed as fin. On the top of silicon the fin nitride has been deposited on a thin pad oxide which protects the silicon fin during gate poly-Si Ge etching . The gates are formed at the vertical sides of the fin using thin gate oxide layer. Gate work function change is essential to adjust the threshold voltage. Hence, for the gate material poly-SiGe has been chosen. The FinFET structure has a uniform front and back metal gate which are attached together and enclosing the conducting channel . This structure gives a better electrostatic control of the gate over a channel. The thin body of the fin is required to ensure that the stand gate has complete control over the channel. The gate come through the wafer plane, current flows in a plane which is parallel to the wafer plane, making the FinFET an quasi-planar structure. FinFETs have an added advantage of the process simplicity and compatibility with the conventional planar CMOS technology. The every process step used to fabricate FinFET is in widespread use today. Another form of gate can also be fabricated on top of the fin, in which it becomes a triple gate FET. Also to an option it can be removed by making the gate oxide thick, so that the channel is formed only in the sides of the fin.

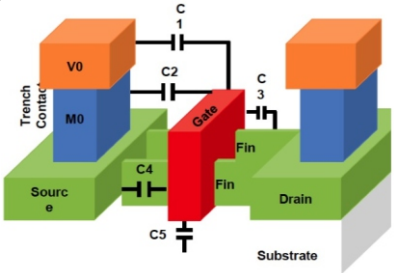



**Figure 1: FinFET Structure**

The important feature in a FinFET is the formation of ultrathin Silicon (Si) fins which forms the transistor channel to reduce the SCEs. A FinFET can have a multiple fins as per the process design. Multiple fins they are usually used to achieve the larger channel width . The dimension of the non-planar device affects the performance in terms of power dissipation and delay.

Figure 2 shows the schematic of a FinFET structure, Where L gate is the physical gate length of FinFET which is defined by the spacer gap, H fin is the height of silicon fin and is defined by the distance between top gate and the buried oxide, T fin is the thickness of silicon fin, and defined by the distance between front and back gate oxides, Next is the extended source or an drain region. The fin width T fin plays a major role for controlling the short channel effect effectively. Therefore, the T fin ~ L gate/2 is followed.

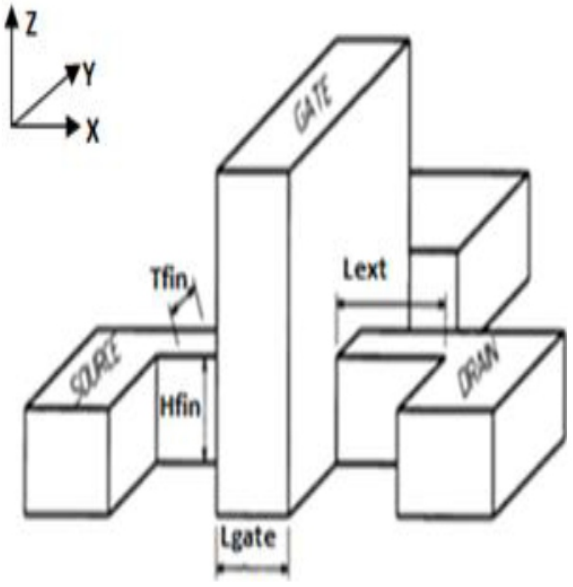



**Figure 2: Schematic of a FINFET Structure**

The basic electrical layout and also the modes of operation of a FinFET do not differ from a traditional field effect transistor. It has one source and one drain contact and also a gate to control the current flow.

### II. Modes of Operations of FinFETs :

Figure 3 shows the FinFET that can be operated in different modes of operations; they are explained in brief here:

#### A. Short Gate (SG) Mode:

In the short gate mode, the front gate and the back gate is shorted together which provides better driving strength. And if one of the input voltages is unstable then either the front gate or the back gate will be able to control over the operation even when the other one is affected. This mode improves efficiency and can achieve low leakage [6].

#### B. Independent Gate (IG) Mode:

The pull up transistors is merged in independent gate mode. The front gate and the back gate are given two independent input voltages respectively. The number of transistors used is reduced, which increases the flexibility in circuit design. The delay is more when compared to ordinary CMOS.

#### C. Hybrid Gate (IG/LP) Mode:

In this hybrid mode, both IG and LP modes are used. Because of this combination, it has the advantageous properties of both the modes. Therefore this makes the mode more advantageous and efficient. The number of transistor used to make this hybrid mode circuit is less in number

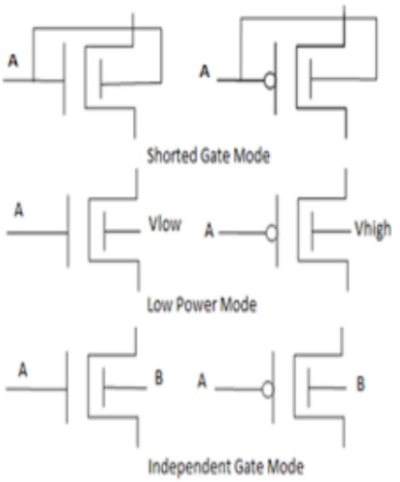



**Figure 3: FinFET – Three Modes of Operation**

### III. Full Adder :

The figure 4 shows a symmetric design which is called as CMOS-Bridge. This design generates Carry and Sum with 20 transistors, here using two inverters for improving the driving capability and produce Carry and Sum. The design uses 24 transistors. The output waveforms are following the truth table1 of full adder.

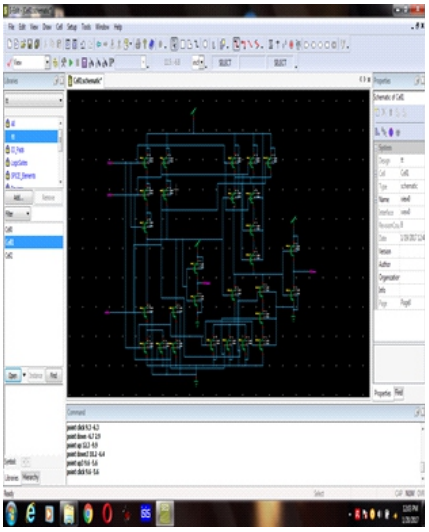


**Figure 4: CMOS-Bridge Full Adder Circuit**

The figure 5 shows a proposed symmetric design and I mplemen tation of Double-Gate Circuit with shorted gate mode which is called as FinFET-Bridge. Full adder is an logical circuit with the three inputs (A, B and Cin) and two outputs that is called Sum and Carry. Full adder is one of the core for the arithmetic processors, therefore by increasing the performance of full adder thereby the performance of processors also increased. The improve in performance which thereby decreasing propagation delay. This design generates Cout and Sum with 20 transistors, the use of two inverters is to improve the driving capability and produce Carry and Sum. Here also the design uses an 24 transistors.

The FinFETs Back gate is used to control the threshold voltage (V T ) of the front gate, which is very important for the performance of the circuit. This is very much helpful in optimization of different circuits in terms of delay, area and power. In this paper we have designed FinFET Full Adder in SG-Mode to obtain a minimum delay and power dissipation in comparison with the CMOS. The waveforms are following the truth table1 of full adder. Here the power dissipation of the circuit in FinFET is least and hence preferred over other CMOS

models. The time taken is less which means the speed is also improved using FinFET.

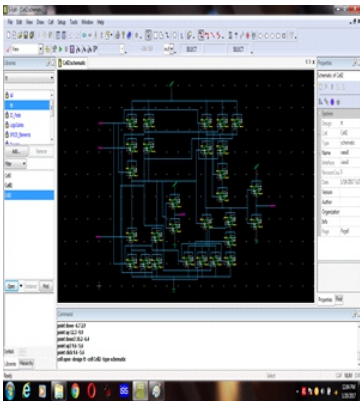


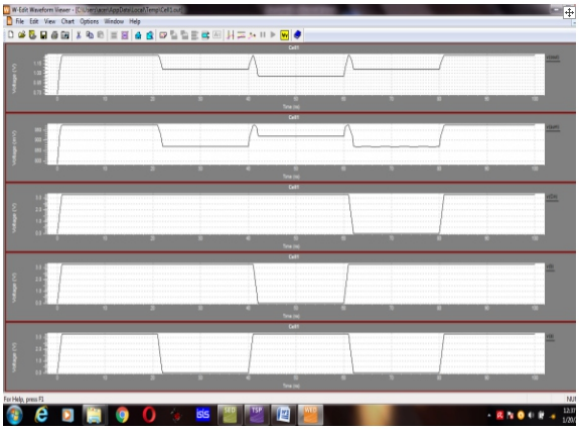
**Figure 5: Proposed FinFET-Bridge Full Adder Circuit using Shorted Gate Mode**

*Truth Table for 1-bit Full Adder*

| Input | | | Output | |
|---|---|---|---|---|
| A | B | Cin | Sum | Cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## IV. Simulation Results and Discussion:

The Simulation waveforms for full Adder using FinFET technology is shown in figure 6. The figure 7 and 8 shows the CMOS technology graph for different I/O bits of full adder versus the delay measurement. The figure 9 and 10 shows the graph for different I/O bits of full adder versus the delay measurement using H spice simulation Tool by selecting FinFET 16nm foundry. The delay and power dissipation for CMOS 32nm and FinFET 16nm technology comparisons has been hereby shown through the graphs and tabulated the differences between them in table2. FinFET technology shows very less power dissipation when compared to CMOS technology in table2. The graphs show that the I/O bits are the output bits sum(S) and carry(C) with respects to the input bits (A, B, Cin). From the graphs we can see that the FinFET graphs shows the minimum variations in delay when compared to CMOS. Compare to the non portable devices, the power consumption is very crucial because of the rising cooling cost and packaging as well as reliability problems. To achieve performance requirements within a power budget was the aims of VLSI (very-large scale integration) designers.



**RESULT OF CMOS BASED FULL ADDER**

**Figure 6: The simulation output for proposed Full Adder using FinFET technology**

**Table 2: Parameter measurements between CMOS and FinFET**

| ABC | Power Dissipation (micro watt) for CMOS 32nm | Power Dissipation (pw ) for FinFET 16nm |
|---|---|---|
| 000 | 1.1012 | 11.0337 |
| 001 | 6.208 | 13.1109 |
| 010 | 6.481 | 12.0759 |
| 011 | 16.933 | 11.1652 |
| 100 | 7.0225 | 10.5927 |
| 101 | 15.4115 | 11.1273 |
| 110 | 14.9081 | 12.2739 |

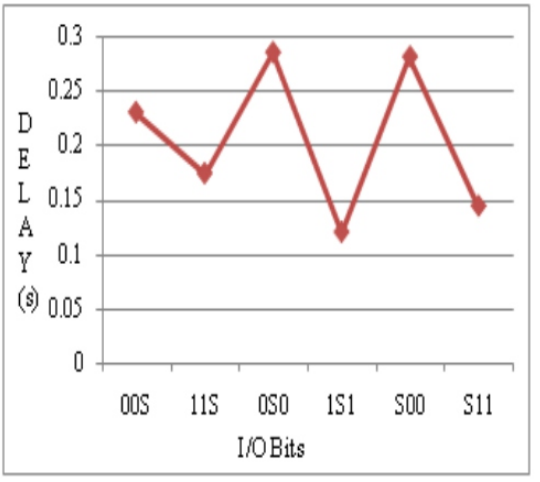



**Figure 7: Graph for Full Adder I/O bits versus delay measurement using CMOS technology**

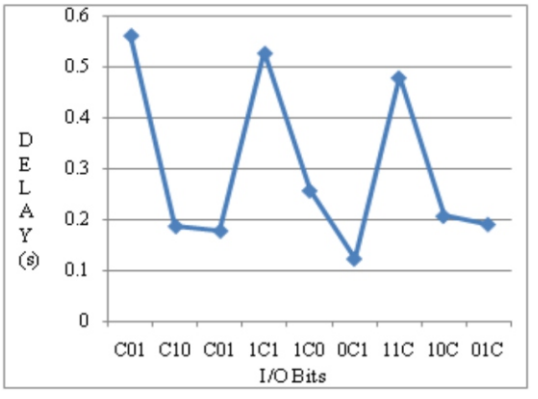



**Figure 8: Graph for Full Adder I/O bits versus delay measurement using CMOS technology**

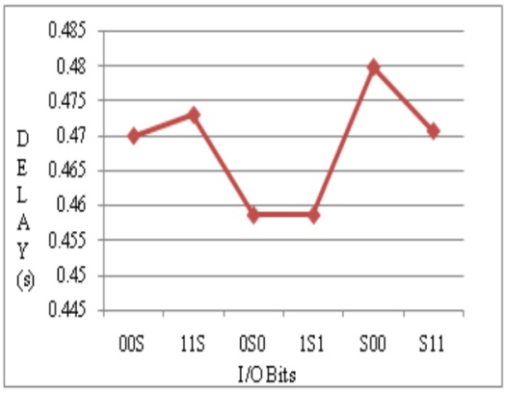



**Figure 9: Graph for Full Adder I/O bits versus delay measurement using FinFET technology**

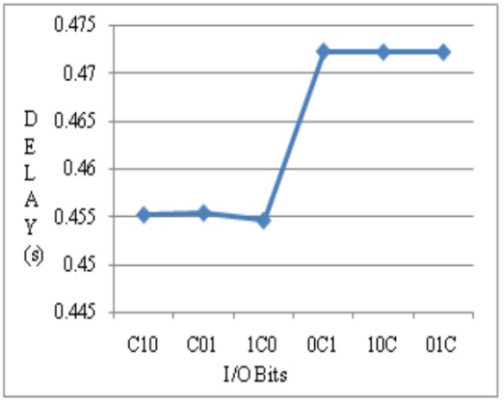



**Figure 10: Graph for Full Adder I/O bits versus delay measurement using FinFET technology**

## I. Conclusion:

FinFET are the new challenge for new material nowadays. This project focussed on the modelling FinFET using a PTM card. Here the FinFET model has been developed by following the parameter from nanoscale design. A new generation of Predictive Technology Model for Multi-gate (PTM-MG) devices has been developed for early-stage design-technology exploration. The DG model of FinFET is successfully constructed and the performance of the device has been analysed. In this paper, FinFET device has been simulated using Tanner tool and waveforms characteristics are plotted. The simulation result shows that with the FinFET, we can get a minimum delay and power dissipation in SG mode. Proposed Bridge-Full Adder is designed in SG-Mode using FinFET technology which is shown in the above circuit diagram, simulated waveforms and tables. By using FinFETs in VLSI circuits power dissipation can be reduced and speed can be improved. By using FinFET technology simulation results like total power dissipation and delay are successfully compared to 32nm CMOS model. Hence we can say that the use of FinFETs in VLSI circuits is essential.

## II. References:

[1] Mahender Veshala, Ramchander Jatooth and Kota Rajesh Reddy, "Reduction of Short-Channel Effects in FinFET," International Journal of Engineering and Innovative Technology (IJEIT) Volume 2, Issue 9, March 2013.
[2] JieGu, John Keane, Sachin Sapatnekarand and Chris Kim, "Width Quantization Aware FinFET Circuit Design," University of Minnesota, Minneapolis.
[3] J. P. Colinge, FinFETs and other Multi-Gate Transistors Springer, 2007.
[4] F. Jafari, M. Mosaffa, and S. Mohammadi, "Designing robust asynchronous circuits based on FinFET technology," IEEE 14th ECDSD, 2011.
[5] International Technology Roadmap for Semiconductors 2010 [Online].Available: http://public.itrs.net
[6] FinFET Circuit Design Prateek Mishra, Anish Muttreja, and Niraj K. Jha.
[7] Mayank Shrivastava, M. S. Baghini, D. K. Sharma, V. R. Rao "A novel bottom spacer FinFET structure for improved short-channel, power-delay, and thermal performance" IEEE Trans. on Electron Devices, vol. 57, no.6, June 2010,pp.
[8] S. Jim Hawkinson, "Analysis and Performance Comparison of CMOS and FinFET for VLSI Applications," International Journal of Emerging Technology and Advanced Engineering ,Volume 3, Issue 2, February 2013.
[9] Masoud Rostami and Kartik Mohanram "Novel dual- Vth independent-gate FinFET circuits" 2010, Digital Object Identifier: 10.1109/ASPDAC.2010.5419680, Page(s): 867 – 872
[10] W. Zhang, J. G. Fossum, L. Mathew, and Y. Du, "Physical insights regarding design and performance of independent-gate FinFETs," IEEE Trans. Electron Devices, vol. 52, no.10, pp.2198-2206, oct. 2005.
[11] S. Sinha, G. Yeric, V. Chandra, B. Cline, and Y. Cao, "Exploring sub-20nm finfet design with predictive technology models," in IEEE International Design Automation Conference, pp. 283 –288, June 2012.
[12] O. Kavehei, M. R. Azghadi, K. Navi, and A.-P. Mirbaha, "Design of robust and high-performance 1-bit CMOS Full Adder for nanometer design," in Symposium on VLSI, 2008. ISVLSI'08. IEEE Computer Society Annual, 2008, pp. 10-15.
[13] Chaudhuri S, Mishra P. and N. Jha K. (2012), Accurate leakage estimation for FinFET standard cells using the response surface methodology, in Proc. 25th Int. Conf. VLSID, pp. 238–244.
[14] Choi J. H, Bansal A, Meterelliyoz M, Murthy J. and Roy K. (2007), Self-consistent approach to leakage power and temperature estimation to predict thermal runaway in FinFET circuits, IEEE Trans. Comput. Aided Des. Integer. Circuits Syst., vol. 26, no. 11, pp. 2059–2068
[15] Chua L. O, Desoer C. A. and Kuh E. S. (1987), Linear and Non-Linear Circuits. New York, NY, USA: McGraw-Hill