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Engineering

AN ULTRA-LOW POWER LNA FOR UWB RECEIVERS USING 90NM CMOS TECHNOLOGY

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ABSTRACT In this paper, An ultra-low-power low noise amplifier (LNA) for ultra-wideband (UWB) receivers is proposed. The configuration doubles the effective gm of the input transistor is the differential inductor feedback structure along with the neutralizing capacitor. In this design, the input device is biased to operate in moderate inversion region to achieve microwatt power dissipation. Experime`ntal results indicate a power dissipation of 70uW, a noise-figure and a forward gain of 18dB. The circuit is designed by using CMOS 90nm process and was powered up using a supply voltage of 1V and also compared with a conventional LNA i.e. without DTMOS. Experimental results show that the proposed LNA exhibits low power consumptions, higher gain, and better linearity.

KEYWORDS :

I.INTRODUCTION

Power minimization is one of the most critical design objectives in wireless integrated circuit (IC) design. Ultra-wideband (UWB) techniques have attracted great interest in both academia and industry in recent years for short range and high speed wireless communication systems. Low noise amplifier (LNA) is one of the most critical blocks in an UWB receiver, because its gain and noise characteristics are closely related to the system sensitivity and dynamic range.

However, it usually requires considerable power to boost the transistor performance. Therefore, many UWB LNAs were developed at the expense of power consumption [4, 5]. This paper will propose an ultra-low-power LNA for UWB receivers. There have been several reported implementations of ultra-low-power RFICs in the last few years [2, 3]. Although these circuits are mainly belong to narrow band circuit and not convenient for the present multi-standard wireless communication system, they also have important directive significance for ultra-low-power UWB RFICs. For ultra-low-power design, the most efficient technological approach to reducing power consumption is to reduce supply voltage and current. Previously, conventional cascade structure [6] has been widely used in LNA circuit to optimize circuit

Performances such as gain and reverse isolation. Nevertheless, it is not suitable for low voltage application as the supply voltage should be twice larger than the threshold voltage (Vth) of the transistors. Reference [7] proposed the folded cascade CS topology can operate at a lower supply voltage of 0.7V, but it induced more branch current and went against the ultra-low-power front-end design. Reference [8] introduced the conventional cascade CS topology which could reduce the supply voltage down to 0.6V, and the gain performance would not be degraded. However, the transistors were working in a weak inversion region, which induced NF and gain performances degradation [9]. However, there are little researchers concentrate on the design of ultra-low-power LNA for multi-standard receivers, especially for UWB systems [12, 13, 14]. In this work, the LNA adopts a resistive shunt feedback topology and a parallel LC load to achieve wideband input impedance matching in 3~10GHz. Furthermore, the LNA circuit deals well with DTMOS technique, and the power consumption is reduced considerably. Some optimized measures help the LNA to improve the power gain and simplify the circuit structure under ultra-low-power consumption.

II. PROPOSED ULTRA-LOW POWER LNA

Fig. 1 shows the schematic of the proposed LNA. The circuit is designed to operate at extremely low dissipation of 70uW.

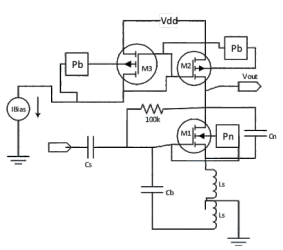

Fig. 1: Proposed ultra-low power LNA With DTMOS

In light of the analytical/experimental study presented in [5], the NMOS transistor *M*1 is biased in moderate inversion region to achieve maximum *gmfT*/*ID*, which corresponds to achieving the maximum GBW for certain amount of bias current. The advantage of using moderately inverted MOSFET is also elaborated in Fig. 2 where the *gmfT*/*ID* is shown with respect to the normalized current, *IN*, for both the analytical model introduced in [5] and the actual measurement results. To further increase the gain at very low bias currents, the proposed LNA also utilizes a *gm*-boosting inductive feedback [6] as well as active load configuration. The inductor feedback forces the gate and source signals to follow each other by 180° phase shift, thereby doubling the voltage gain. Moreover, by making the neutralizing capacitor *CN* equal to *CGD* of the input device, *M*1, the differential inductor feedback will also neutralize the *CGD* effect, which is critical in LNA circuits not using cascade structure [7]. A 100kΩ resistor in a local shunt feedback configuration between the gate and drain of *M*1 is used to bias the circuit. It is readily shown that the value of the bias resistor has to be chosen sufficiently large so as to eliminate its impact on the gain degradation of the proposed LNA.

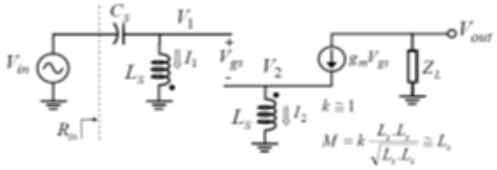

Fig.2: Small signal model for Cgd

Using the voltage and current equations of the differential inductor and assuming that coupling factor k to be close to unity, it is easily proved that the gate and source voltages follow each other with a 180° phase difference. The voltage gain of the LNA is thus expressed as

$$A_v = -g_m V_{gs} Z_L = -2 g_m V_1 Z_L \qquad (1)$$

Equation (1) indicates that the differential inductor doubles the gate-source voltage compared to a simple common-gate or common-source LNA, and therefore, the transistor's *gm* effectively increases by a factor of two. The driving-point impedance of the proposed LNA is calculated from Fig. 2, which results in eq (2)

$$Z_{in}(j\omega) = \frac{1}{j\omega C_S} + j\omega L_S + \omega^2 L_S^2 2 g_m \qquad (2)$$

DTMOS logic

From the past few years due to the extensive growth of market for portable devices such as cell phones, portable computers, other low power applications and also the design of analog circuits which requires low power, low voltage with high performance has become an important issue now a day's. One of the limitations for implementation of portable devices and design of other low power circuits at low voltage is the threshold voltage (Vth). For this reason reduction of threshold voltage is necessary for low-power, low-voltage operation.

DTMOS technique [9] is the best solution for reduction of threshold voltage (Vth). Therefore, an effective method for reducing power consumption is to reduce the power supply voltage (V_{dd}). So the reduction of power supply voltage (V_{dd}) depends on one of the factor that is threshold voltage. So one of the possible solution is to implement CMOS transistors with dynamic V_{th}, which is the basic idea behind DTMOS technique. DTMOS transistor shows high threshold characteristic when it is in "off" condition to minimize the leakage current as well as, it behaves as a low threshold device in "on" condition at lower supply voltages for high current driving capability. This is one of the feature that makes DTMOS technique most suitable for low-voltage, low power applications.

In dynamic threshold CMOS (DTMOS), the threshold voltage is altered dynamically to suit the operating state of the circuit is shown in figure 3, here the NMOS and PMOS transistor body is biased dynamically. Sufficient body biasing voltage to both PMOS and NMOS transistors are provided by the potential dividers (pd) which are connected to the input of the inverter. A high threshold voltage in the standby mode gives low leakage current, while a low threshold voltage allows for higher current drives in the active mode of operation. Dynamic threshold CMOS can be achieved by tying the gate and body together. The supply voltage of DTMOS is limited by the diode built-in potential in bulk silicon technology. The pn diode between source and body should be reverse biased. Hence, this technique is only suitable for ultralow voltage (0.6V and below) circuits in bulk CMOS.

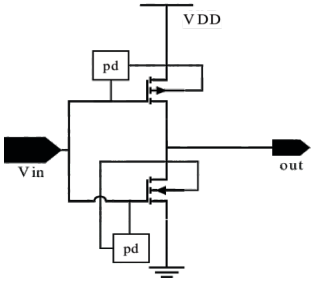

Fig.3 DTMOS Circuit

The DTMOS [10] technique reduces the transistor off-state leakage current as well as reduces the threshold voltage during on-state (VBS> 0). After fabrication, the threshold voltage (V_{TH}) of transistors can be modulated by changing the body-to-source voltage. In bulk MOSFETs, the V_{TH} is given by:

$$V_{th} = V_{th} + \gamma\left(\sqrt{|2\emptyset f - V_{BS}|} - \sqrt{|2\emptyset f}\right)$$

Where
Vth is the threshold voltage,
Vth0 is threshold voltage for VBS=0,
γ is the body effect factor that ranges from 0.3 to 0.4, φf is the Fermi potential with a typical value in the range of 0.3 to 0.4V.

III. MEASUREMENT And RESULTS

The LNA circuit has been designed using CMOS 90nm process. The circuit operates at the center frequency of 2GHz with total power dissipation of 70uW from 1V supply. A source follower buffer was placed at the output of the amplifier to avoid the loading effect of the measurement devices at the high impedance output of the LNA circuit. The buffer was also fabricated separately, and the final measurement results were derived by de-embedding the effect of the source follower. The de-embedding was achieved by measuring the NF and gain of the buffer separately. To improve the accuracy of the S_{12} measurement. The input return loss S_{11} and the reverse gain S_{12} were measured using spectre simulator the LNA exhibits an S_{11} are shown in Fig.4, the measured S_{12} is compared with the simulated S_{12} of the circuit without the neutralizing capacitor C_N.

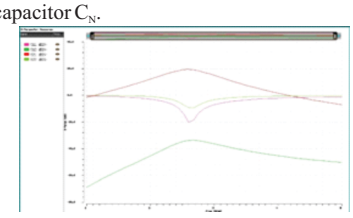

Fig.4: LNA s-parameters plots

The measured NF and gain of the LNA are shown in Fig. 8. The results were calculated from the measured data for the combination of the LNA and buffer, and by deem bedding the buffer effect from the measurement result. The proposed LNA exhibits a NF of 3.9dB and a small signal voltage gain of 18dB at the RF frequency of 2GHz. Results of the gain for the LNA is shown in Figs. 5.

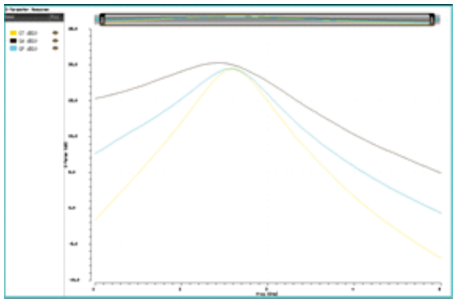

Fig 5. GT, GA, and GP

Table 1 shows the summary of the measurement results of both circuits. As evident from Table 1, the power optimization of the LNA is improved by using DTMOS technique. Finally, compared to the latest prior work presented in [11], the circuit exhibits lower power consumption, higher gain, and better NF.

Table1: Performance comparision

Parameter	Proposed LNA	conventional LNA
Supply voltage	1V	1V
DC current	70uW	100uW
Operationa freq	2Ghz	1Ghz
Voltage Gain	18dB	16.8dB
Noise Figure	2.8dB	3.9dB

IV. CONCLUSIONS

An ultra-low power LNA with inductive feedback and DTMOS architecture was designed in a CMOS 90nm process operating at 2GHz. Using the neutralizing capacitor, it was shown both analytically and experimentally that this structure cancels the effect of *CGD* capacitor. The actual measurement results have shown a small signal gain of 18dB with a power dissipation of only 70μW. Moreover, the comparison between the proposed LNA and a conventional LNA with the less power dissipation proves the good performance of the proposed LNA.

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