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# FSM based FPGA Design for Digital Demodulation

KEYWORDS: Phase lock loop(PLL),ROM, Finite state machine(FSM),Binary phase shift keying, Field programmable gate array(FPGA).

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**ABSTRACT** This paper is concern with hardware design of digital demodulation using an Altera Programnable device.The binary phase shift keying(BPSK) demodulator is designed. The detection logic for BPSK demodulator is designed using Bit detection logic finite state machine. Two IP cores PLL and ROM are used for the purpose of synchronization and storing samples of modulated bit stream. This demodulation method can greatly improve the developing efficiency, shorten developing period for implementation on FPGA. Results of theoretical simulation(MATLAB) and practical engineering(Modelsim) are same. This Paper also highlights the programmable nature of the design.

## I. INTRODUCTION

THE aim of this paper is to design BPSK demodulator at low bit rate for altera satrixIII FPGA board.Modulated bit stream is stored in ROM megafunction and bit stream is user controllable. Demodulation is done by using coherent detection technique in which knowledge of phase and carrier frequency must be known to receiver and it can be achieved by using PLL at receiver side. A PLL essentially locks to the incoming carrier frequency and tracks the variation in frequency and phase. Assume that carrier phase recovery is done and simply use generated reference frequency at receiver then in coherent detection technique reference signal is multiplied by a reference frequency generator and a threshold detector makes a decision on each integrated bit based on a threshold.[3]

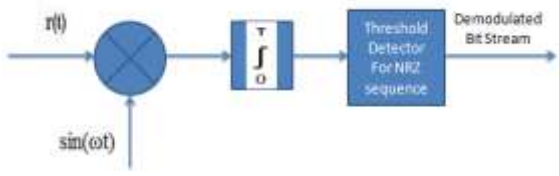


**Fig. 1. Basic concept of coherent detection technique[3]**

Basic concept of coherent detection technique is shown in Fig.1.Since an NRZ sequence is used with equal amplitudes in positive and negative direction, the threshold for this case would be "0".[3] First BPSK demodulation is simulate in Matlab then we compare results for FPGA design using Altera Modelsim with Matlab simulation results.Fig.2 shows Basic concept of BPSK demodulation which is designed in Matlab. This is designed is such that all the input parameters carrier frequency,sampling frequency,Bitrate and Input bitstream can have variable values, thus making it a generic BPSK demodulator.In a matlab function all these parameters are passed as input to demodulator.

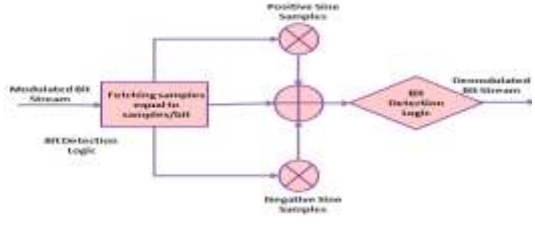

**Fig. 2.Basic concept of BPSK demodulation technique**

Then samples per sine wave required, it can be obtain by dividing the 0 to 360 degrees in that no of values for representing 1 sine wave. For example if it is 5, then we get [0,72,144,216,288,360]values in between 0 to 360.Then take sine of all above values and store it in an array making 1 sine wave to represent modulated bit 1 while take –sine of all above values and store it in another array making 1 sine wave which is 180 degree phase shifted to represent modulated bit 0.Then create two arrays in which in we append sine waves per bit times the array representing 1sine wave to get 1 bit modulated sinewave signal for bit 1 and for bit 0.

From input modulated bit stream we fetch values equal to number of sample per bit and store it in an array. Then multiply the above array containing samples of BPSK modulated bit with the two arrays representing modulated bit 1 and bit 0.Each element of the multiplied output of both array are summed in two respective variables. Then bit detection logic is used for detecting whether bit 1 or 0 is detected. [3]

## II. FPGA DESIGN FOR BPSK DEMODULATION

In BPSK demodulation we have used two Altera Megafunctions. They are PLL and rom_sine_samples_d.PLL is used to convert the board clock of 125 MHz to 120 MHz, used in entire design. Rom_sine_samples_d is a Rom 1 megafunction which has 50 thousand sine wave samples of 14 bits, making 5 modulated bits that is 10 thousand sine wave samples per modulated bit.

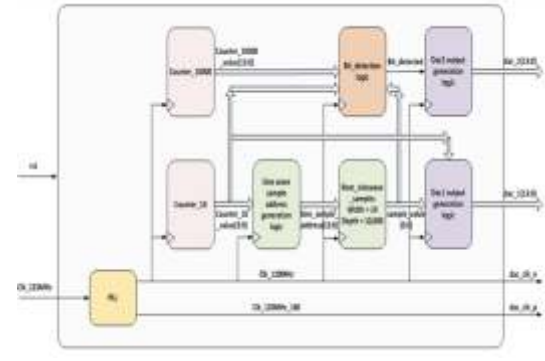

**Fig.3.FPGA design for BPSK demodulation**

As we also know from modulation that 1 bit prevails for 1 lakh counter and we have 10 thousand sine wave samples per bit, so here also we design a counter_10 which is modulo 10

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counter.Whenever the counter_10 value is 10, sine wave sample address generation logic increments the address to the rom_sine_samples_d by 1 thus fetching 1 sample. Thus 10 thousand samples are fetched in 1 lakh clocks.Once all the 50 thousand samples are fetched, sine wave sample address generation logic starts fetching samples from 0thlocation.Sine wave samples out from the rom_sine_samples_d are given to bit detection logic.

Since we can have minimum of 1 sine wave per bit in modulation process and that accounts for 10 thousand samples, we designed a counter, counter_10000 that can count maximum up to 10000.[1] We have defined a constant in design, to which user puts the value of no of samples per sine wave used in modulation process. Constant can have maximum of 10000 value as it accounts for 1 sine wave per modulating bit.Counter_10000 counts up to constant having the value of no of samples per sine wave and then roll over and starts counting from 0.Counter_10000 and counter_10 are also inputs to bit detection logic along with Sine wave samples out from the rom_sine_samples_d.[1]

Bit detection logic demodulates the modulated input samples and gives the detected bit out.If bit detected is 1 then Dac2 output generation logic gives all 1 in 14 bit output and if it is 0 then it gives all 0 in 14 bit output to DAC2.Dac1 output generation logic gives directly the samples out from the rom_sine_samples_d to the 14 bits of Dac1.Thus demodulated bit we get from dac2 and input BPSK modulated signal we get from dac1 output.

## III. BIT DETECTION LOGIC FINITE STATE MACHINE

Bit detection logic is a control FSM with 3 states: start, detect and smpl_cnt_inc. Fig.4. shows bit detection logic using three FSM states. FSM output is the demodulated bit while inputs are modulated sine wave samples, counter_10 and counter_1000. The states and their functioning are explained in detail below.

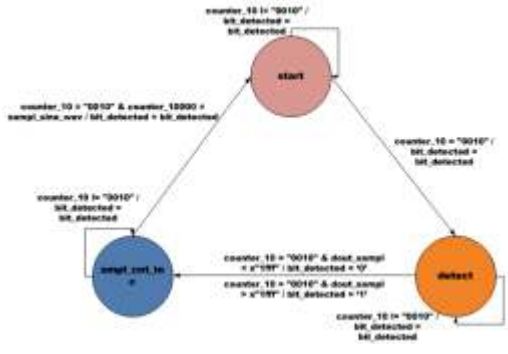


**Fig.4.Bit detection logic FSM**

**Start:**
On power on or during reset the fsm is in this state. Rom_sine_samples_d takes 2 clocks, after its address is incremented by sine wave sample address generation logic to get its new sample value out. So when counter_10 value is 2 we have a new sample value out.Therefore on power up or on reset or when samples equal to 1 sinewave have been fetched out, first sample of a sinewave is out from the rom_sine_samples_d when counter_10 has value of 2. Fsm jumps to the detect state on this condition.

**Detect:**
In this state we detect the bit is 0 or 1. The second sample fetched is compared with hexadecimal 1fff, if it is greater than that, our sine wave is going in positive cycle and if it is lesser than that, our sinewave is going in negative cycle. So if its going in positive cycle we conclude that bit is 1 else its 0 and FSM jumps to smpl_cnt_inc.

**Smpl_cnt_inc:**
In this state FSM waits until all samples for 1 sinewave are fetched. It increments the counter_10000 on every sample fetched from rom_sine_samples_d and compares it with the constant value samples per sine wave. When counter_10000 equals the constant value FSM jumps to start state to begin the process again for next sine wave samples.

## IV. SIMULATION RESULTS

Fig.5 & fig. 6 shows Matlab simulation results when bitrate is respectively 120bps and 1200bps.In fig.5. carrier frequency is 1200Hz and sampling frequency is 9600Hz.In fig 6. carrier frequency is 48Khz and sampling frequency is 12000Khz.

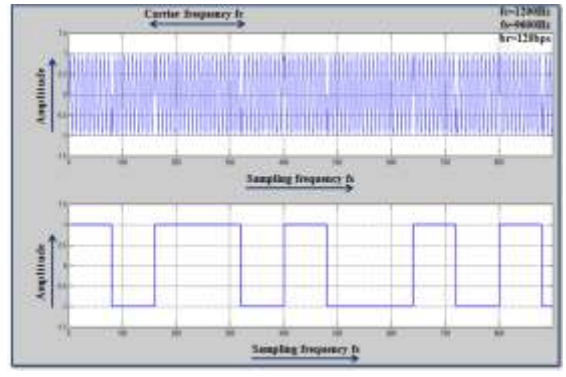


**Fig.5. BPSK demodulation results when bit rate is120bps**

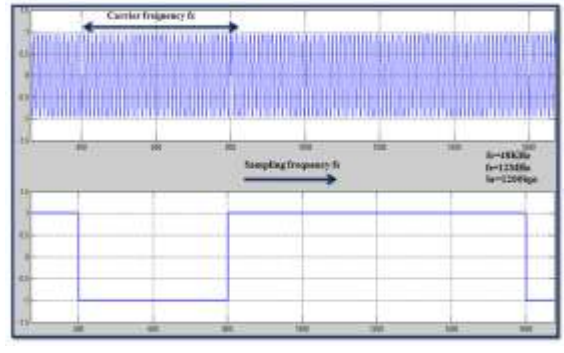


**Fig.6 BPSK demodulation results when bit rate is1200bps**

Both figure shows theoretical results of BPSK demodulation at different bit rate, carrier frequency and sampling frequency. These results are finally compared with practical FPGA design results in modlesim for checking functionality of design.

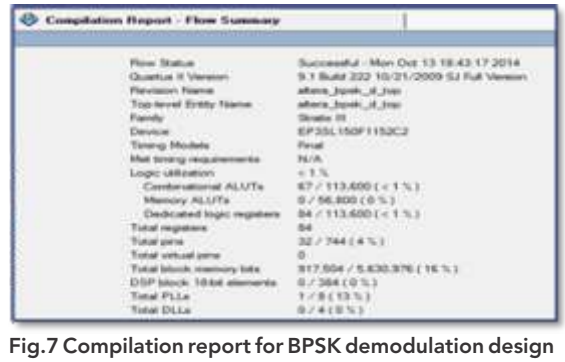


**Fig.7 Compilation report for BPSK demodulation design**

Fig.7 shows compilation report of BPSK demodulation which shows compilation status is successful and also gives total

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number of pins ,components &LUTs used on stratixIII FPGA board in design part.

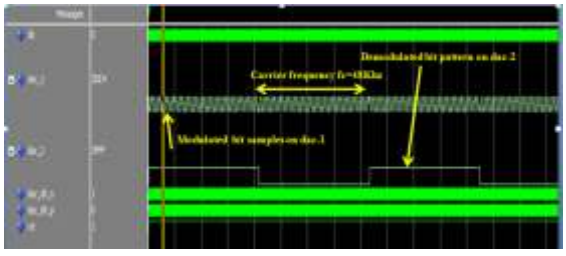


**Fig.8 BPSK demodulated wave when bit rate is equal to 1200 bps**

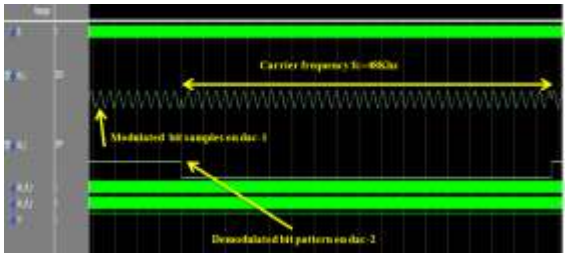


**Fig.9 Zoom in view of BPSK demodulated wave when bit rate is equal to 1200 bps**

Above waveforms in Fig.8 & fig.9 shows demodulation of 40 sinewave representing 1 bit. Waveform dac signals in analog format, which shows carrier frequency is equal to 48Khz.

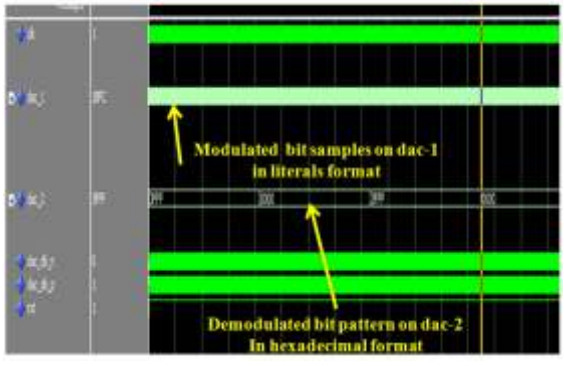


**Fig.10 BPSK demodulated wave in literal format**

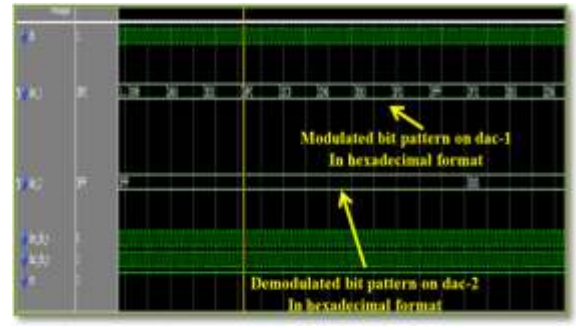


**Fig.11 BPSK demodulated wave in hexadecimal format**

Above waveforms in Fig.10 & 11 shows the same demodulation with format literal and samples from rom_sine_samples_d in hexadecimal form.

## V. CONCLUSION

In this paper FPGA design technique for digital demodulation is introduced and we can see that results of theoretical simulation(MATLAB) and practical engineering(Modelsim) are same, it means design is working properly. This paper gives detail description to design bit detection logic finite state machine which is main part in FPGA design of BPSK demodulator. This demodulation method can greatly improve the developing efficiency, shorten developing period for implementation on FPGA.

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