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Design Of Optimised Multiplication Technique Using Column Bypass Multiplier

KEYWORDS: Area efficient, column bypass multiplier, reduced power consumption, twin precision.

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ABSTRACT The performance of the embedded system, microprocessor and many DSP applications are mainly dependent on the performance of the multiplier. The use of conventional full precision multiplier results in increase in the power, area and computational time. Hence multipliers are the basic key element of any computational unit responsible in decreasing the power as well as increasing the speed. In this work, review of different multiplication techniques is described and at last the proposed method which will be modelled using VHDL.[1]-[7]

I. Introduction

MULTIPLICATION is a complex arithmetic operation, which is reflected in its relatively high signal propagation delay, high power dissipation, and large area requirement. When choosing a multiplier for a digital system, the bitwidth of the multiplier is required to be at least as wide as the largest operand of the applications that are to be executed on that digital system. The bitwidth of the multiplier is, therefore, often much larger than the data represented inside the operands, which leads to unnecessarily high power dissipation and unnecessary long delay. This resource waste could partially be remedied by having several multipliers, each with a specific bitwidth, and use the particular multiplier with the smallest bitwidth that is large enough to accommodate the current multiplication. Such a scheme would assure that a multiplication would be computed on a multiplier that has been optimized in terms of power and delay for that specific bitwidth. However, using several multipliers with different bitwidths would not be an efficient solutions, mainly because of the huge overhead.[1]

Narrow-width operands have also been used to increase instruction throughput, by computing several narrow-width operations in parallel on a full width data path, Loh showed a 7% speedup for the SPECint2000 benchmarks by using a simple 64 bit ALU, which excluded the multiplier , in parallel with four simple 16-bit ALUs that share a 64-bit routing. Brooks did a similar investigation, where they envisioned a 64 bit adder that could be separated into four 16 bit adders by serving the carry chain.[5]

M. Sjalander, H. Eriksson, and P. Larsson-Edefors presented the twin precision technique[2] that offers the same power reduction as operand guarding and the possibility of performing double-throughput multiplications. The twin precision technique is an efficient way of achieving double throughput in a multiplier with low area overhead and with only small delay penalty. We show how to apply twin precision technique on signed multiplier based on the column bypass multiplier.[2]

II. Literature review

1) Multiplication acceleration through twin precision[2]-[5]

In this paper it is presented that the twin precision technique allows for flexible architectural solutions, where the variation in operand bitwidth that is common in most applications can be harnessed to decrease power dissipations and to increase throughput of multiplications

It turns out that the Baugh-Wooley algorithm implemented on a HPM reduction tree is particularly suitable for a twin precision implementation. Due to this simplicity of the implementation, only minor modifications are needed to comply with the twin precision technique. This makes for an efficient twin precision implementations capable of both signed and unsigned multiplications.[1]

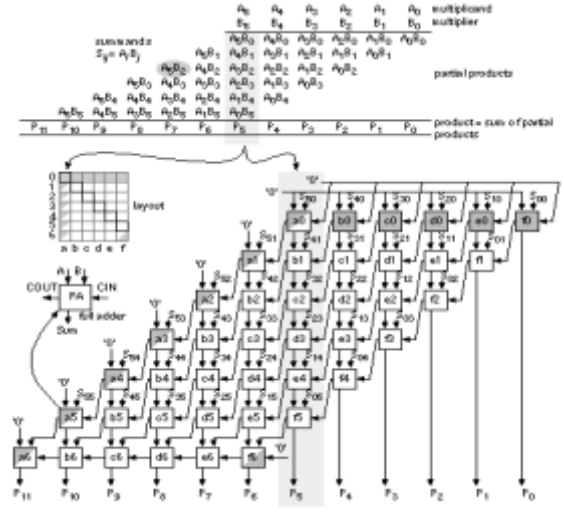

Fig. Illustration of unsigned 8 bit multiplication.

2) Low power reconfigurable multiplier with reordering of partial products[8]

In this paper the author proposed reordering of partial products technique for modified DADDA and modified HPM unsigned multipliers. The results showed that modified HPM has less power consumption than the modified DADDA and basic HPM. The modified DADDA is not preferred for twin precision type of multiplications. The ordering of partial products can be applied to the signed multipliers also.[1]-[3]

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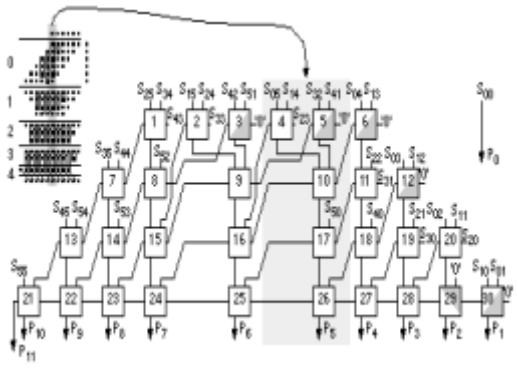


Fig. Dadda multiplier

3) Delay optimised 16 bit twin precision Baugh Wooley multiplier[9]

In this paper the author presented that the twin precision technique allows for flexible architectural solutions, where the variations in operand bitwidth that is common in most applications can be harnessed to decrease power dissipation and increase throughput of multiplications. It turns out that the Baugh Wooley algorithm implemented on HPM reduction tree is particularly suitable for a twin precision implementation. Only simple modification needed which makes an efficient implementation capable of both signed and unsigned multiplications.[1]-[9]

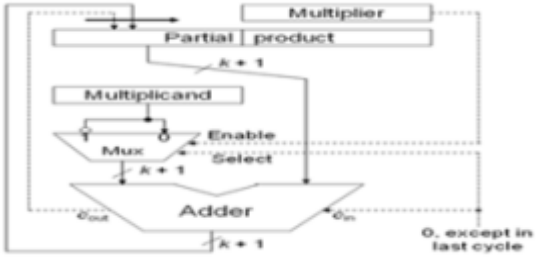


Fig. Block diagram of BW algorithm

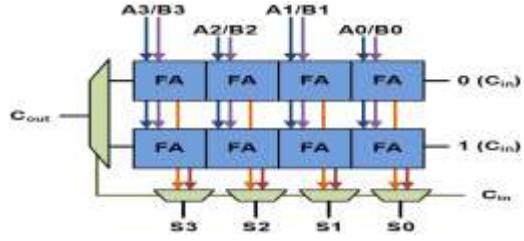
III. The Proposed design

The main aim of the design is to reduce the power, delay and make the the multiplier work faster. The activity of switching in any circuits depends upon the input bit coefficient. This depicts that if the input bit coefficient is zero then the corresponding row or column need to be activated. If more numbers of zero in the multiplicand then higher power reduction can be achieved. The proposed design depicts to use column of carry select adder for bypassing by approaching this the operations in a column can be disabled if the corresponding bit in multiplicand is zero.The carry select adder generally consists of two ripple carry adder and a multiplexer. The number of bits in each carry select block can be uniform, or variable. [1]-[7]

Tools Used:

We used XILINX ISE v 10.2 for our programming. We considered VHDL as our primary language. For test bench waveforms also we also used Xilinx to write our own test benches. Model Synthesis Map report all features in Xilinx helped us a lot.

We used Xilinx's XPower Estimator (XPE) tool in order to calculate power consumed in any arithmetic circuit. For calculation of power using Xilinx's XPE we need to generate the map report file in XILINX which will be saved in the same directory with an extension ".mrp". But in the later part of the project we used SYNOPSIS tool for finding out Power and delay and Area calculations.



IV. Conclusion

In this paper, literature review of different paper along with their proposed techniques have been depicted. Baugh Wooley, modified booth algorithms, modified DADDA and basic HPM are used to make a processor more efficient, and at last the proposed design of column bypass multiplier along with the tools to be used and the basic building block is shown.

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