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FinFET – A Substitute of bulk-Si MOSFET in Nanometer Regime

KEYWORDS

Mitesh Limachia
Asst. Professor, EC, DDUniversity, Nadiad

Chirag Makwana
Lecturre, Dept. of Engg and Enterprise, IIAR

Dr. Nikhil Kothari
Professor and Head, EC, DDUniversity, Nadiad

ABSTRACT To continue MOSFET technology downscaling, short channel effects need to be effectively suppressed in nano-scale devices. By using double gates to modify the single-gate MOSFET structure, FinFETs have suppressed SCEs more effectively than other counterparts and appeared as a promising substitute in future technology beyond 22 nm. A tied gate of FinFET achieves higher performance while isolated gate of FinFET offers rich design options. In this paper, we present study of FinFET architecture and demonstrate effectiveness of FinFETs in static, dynamic and memory configurations. Performance of FinFET configurations is compared with bulk-Si MOSFET implementation in terms of delay, on-state and off-state power.

I. INTRODUCTION

MOSFETs are still acting as a dominant device in VLSI due to numerous advantages [1]. Motivated by increasing interest of high speed, small size, battery-operated portable appliances, the steady miniaturization of MOSFETs with new generation of technology provided enhanced circuit performance during the last decade. However, downscaling of MOSFETs becomes substantially difficult below 32 nm technology scale due to several effects [2]. They are identified as (i) severe short channel effect (SCE) (ii) random dopant fluctuation (RDF) (iii) parametric variations (iv) non-negligible parasitic components (v) quantum mechanical effects [3].

Major challenge in continuing the Moore's scaling lies in controlling SCE. Proximity of source and drain reduces control of the gate over the channel and the threshold condition can be reached at a lower gate turn on voltage [4]. This results in (i) VT roll-off leading to exponential increase in off-state current IOFF and unacceptable channel length [5]. (ii) Drain Induced Barrier Lowering (DIBL) effect causing lowering of VT and increases IOFF as well as change in subthreshold swing [6]. Hence, while designing transistor in nanometer regime, along with drive current ION, IOFF should be optimized [7].

Approaches for overcoming such effects have physical limitations in nanometer regime due to increasing fabrication complexity and cost [8]. Suppression of SCEs demands new architectural devices for better yield. FDSOI, FinFET, triple-gate and GAA have been proposed to improve scalability [9]. Among these, FinFETs are considered an attractive option because of good scalability, easy integration into existing CMOS fabrication process and better electrostatics using dual-gate architecture [10].

This paper presents a comprehensive study combined with performance evaluation of different digital systems with FinFETs based implementation. The study summarizes utilization of FinFETs in various circuit configurations. Application of FinFETs is implemented and simulated for static, dynamic and memory configurations with performance comparison.

II. ISSUES IN SHORT CHANNEL DEVICES

In a short-channel device, channel region is influenced by source/drain as much as by gate, shifting conduction band edge near the source end of channel (Fig. 1). The shift represents an effective lowering of the barrier between source and channel. As a result, electron moves from source to drain with ease in off state leading to high IOFF. Additionally, due to barrier lowering (drain induced barrier lowering DIBL), device can conduct at a lower gate turn on voltage and reduce VT. Strong DIBL indicates (i) poor short-channel behavior and (ii) degraded device characteristics such as VT roll-off and high IOFF. With technology downscaling, reduced VT increases IOFF and static power dissipation. Heavy channel doping (> 10 18 cm-3) or halo implants are modifications in MOSFET technologies to enhance VT and suppress SCEs [11]. However, impurity scattering in channel area (random dopant fluctuation) severely degrades carrier mobility in such approaches resulting poor ION and delay performance.

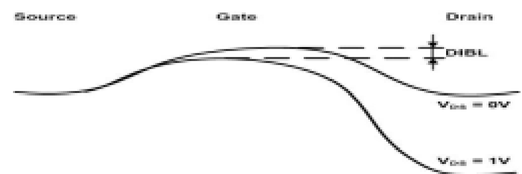

Fig. 1 Conduction bend profile in channel region

While fabricating MOSFET on ultra-thin body SOI is an effective approach for better electrostatic control of gate. SOI is expensive as compared to conventional silicon substrate [12]. t_{ox} cannot be scaled beyond a certain limit because of increasing tunneling effect and tunneling current associated with smaller t_{ox}. These limitations led to new architectural devices with better electrostatic control of gate proposed for suppression of SCEs and better yield.

FDSOI, FinFET, triple-gate, GAA with light channel doping have been proposed to suppress SCEs [13]. VT is a sensitive function of channel thickness (< 5 nm), which suffers from quantum mechanical effects and makes difficult to scale FDSOI technology beyond 22 nm [14]. Tripple-gate devices have relatively poor layout efficiency compared to double gate devices [15]. GAA devices offering near-ideal channel control are expensive to manufacture [10]. Double gate

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devices, such as FinFET achieve good SCEs behavior with less stringent body thickness requirement [12].

III. FINFET- DEVICE TECHNOLOGY

FinFET, a vertical double-gate structure (Fig. 2) consists of a channel formed in a vertical Si fin controlled by a self-aligned double-gate [16]. FinFET is fabricated by etching a thin fin of silicon through SOI layer. Vertical fin can be manufactured with conventional lithography and etching [17]. Thus, FinFET fabrication is easily integrated into CMOS fabrication without additional masking. Effective width (W) of FinFET determined by Eq. (1) allows wider transistor with higher on-current requirement using multiple parallel fins. Increasing H_{fin} instead of W_{fin} increases device on-current without increasing channel width [5].

$$W = 2 * n * H_{fin} + t_{si} \quad (1)$$

Fig. 3 shows modeling of parametric details of FinFET device architecture. Table 1 shows parameters important for minimizing IOFF and maximizing ION in 45 nm. With smaller tox, Cox between gate and substrate improves to increases electrostatic control over channel and restrict VT fluctuations. Since, FinFETs enable better performance due to second gate they do not need high channel doping for high VT. Less channel doping minimizes the effect of RDF on VT variations as expressed below.

$$\sigma\Delta V_T, RDF = tox/\varepsilon ox \cdot (4\sqrt{2q3\varepsilon siNa\varphi B}) / \sqrt{3WeffLeff} \quad (2)$$

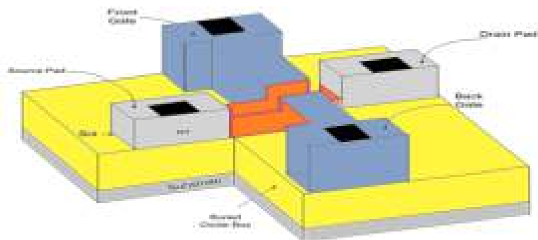


Fig. 2 FinFET structure

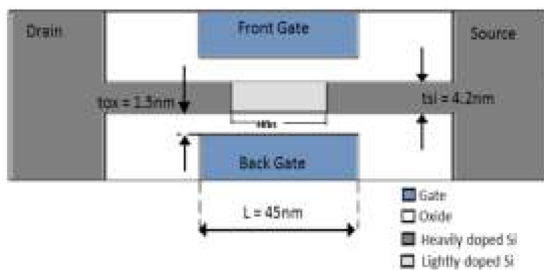


Fig. 3 Cross-section view

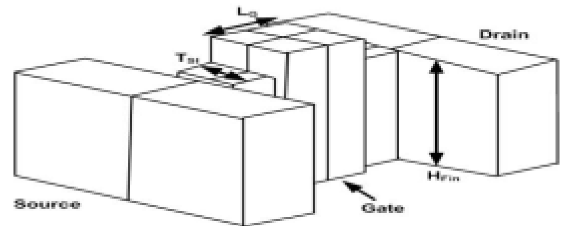
TABLE 1 PARAMETRIC DETAILS

Channel Length (L)	45nm
Fin Thickness (t_{si})	4.2nm
Fin Height (H_{fin})	45nm
Oxide Thickness (t_{ox})	1.5nm
Channel Doping (N_{ch})	2×10^{16} cm^{-3}
Source/Drain Doping (N_{SD})	2×10^{20} cm^{-3}

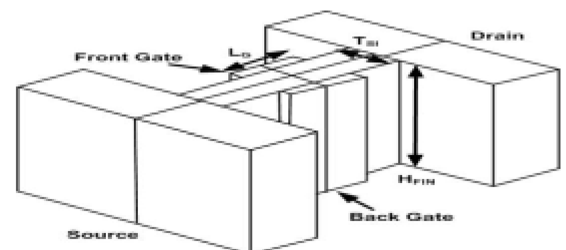
Two electrically coupled gates along with thin silicon body (t_{si}), where current conduction takes place, suppresses SCEs [18]. Thicker t_{ox} and thinner t_{si} are preferred to increase t_{ox}/t_{si} ratio, and larger ΔV_T is accomplished. This large V_T variation is favorable for balance between switching speed and I_{OFF} control.

I. FINFET MODES

In Shorted-Gate (SG) FinFETs, two gates are connected together (Fig. 4). This could be a direct replacement of conventional CMOS devices. In Independent-Gate (IG) FinFETs, front and back gates are separated by oxide on top of the silicon fin (Fig. 4) creating two independent gates with more options [19].



(a) SG-mode



(b) IG- mode

Fig. 4 FinFET modes

With appropriate independent bias conditions, IG-FinFET can be operated in: (i) In dual gate mode, front and back gates are biased with same signals. (ii) In single gate mode, one gate is biased with input signal to form channel inversion with other gate disabled [19]. Strongly coupled gates in dual-gate mode lower V_T as compared to other mode for higher performance. Dynamic V_T tuning of single gate mode reduces I_{off}.

I. FINFETS APPLICATIONS

FinFETs are preferred to implement static (small fan-in gates), dynamic (wide fan-in gates) and memory configurations as shown in Table.2. SG-mode and IG-mode (double gate) are used to implement static gates to achieve higher circuit performance. IG-mode (single gate) is preferred in domino gates for improving power consumption vs. delay trade-off. In domino circuit configurations, keeper transistor is typically smaller (to obtain small V_T) than evaluation transistors in order to minimize delay and power degradation caused by keeper contention [20]. A small keeper (small V_T) cannot provide the required noise immunity. V_T of keeper transistor is dynamically modified (IG- mode) during circuit operation by varying back gate biased to reduce contention without sacrificing noise immunity. This is especially useful in SRAM configurations to obtain improved SNM vs. access time trade-off.

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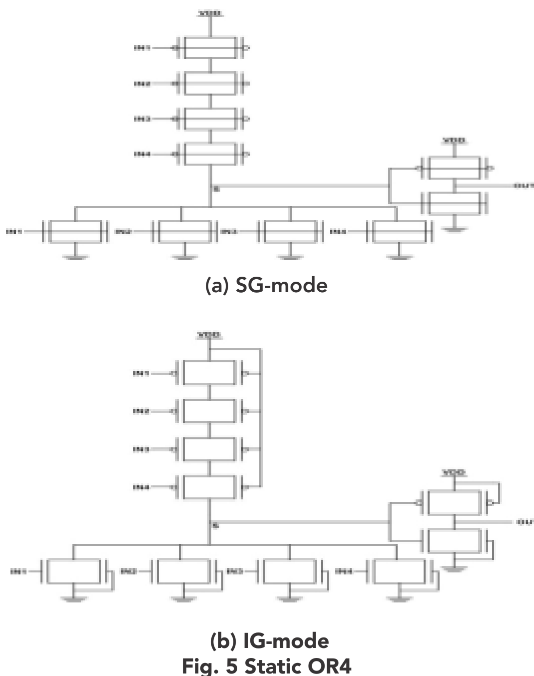
TABLE 2 FinFET UTILIZATION

Implementation	Technique	FinFET Modes			
		SG	IG (dual gate)	IG (single gate)	Mix
SRAM cell	Flex-PG [21]	√	√	×	√
	Flex-V_T [22]	×	√	×	×
	PGFB [23]	√	√	×	√
	32K 6-T SRAM Array [24]	×	√	×	×
Domino gates	Dynamic V_T tuning of keeper [25]	×	√	×	×
	4T- FinFET in dual role [26]	×	√	×	×
	Dual role of symmetric 4-T FinFET [18]	×	√	×	×
	V_T tuning by clock at back gate of transistors [27]	×	√	×	×
Static Gates	NAND gate [28]	√	√	√	×
Seq. circuits	latches with dynamically controlled V_T [29]	×	√	×	×
	Latches using 3-T and 4-T FinFETs [29]	√	√	×	×

VI. FINFET IMPLEMENTATION OF CIRCUIT CONFIGURATIONS

Implementation of OR4 gate using SG-mode and IG-mode (single gate) is presented in Fig. 5. Fig. 6 shows domino OR8 using IG-mode. Combined precharge and keeper Dual purpose FinFET devices reduce clock and load capacitance leading to lower on-state power and delay [20].



(a) SG-mode

(b) IG-mode

Fig. 5 Static OR4

Fig. 7 shows 6-T SRAM cell using IG-mode (single gate). Disabled back gates of p-type and n-type FinFETs increase the absolute V_T of front gates. Rise in V_T reduces I_{OFF} and improves noise immunity with less off-state power. It leads to degradation in circuit delay with performance trade-off.

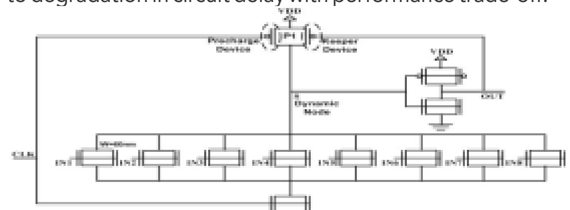


Fig. 6 Domino Or8

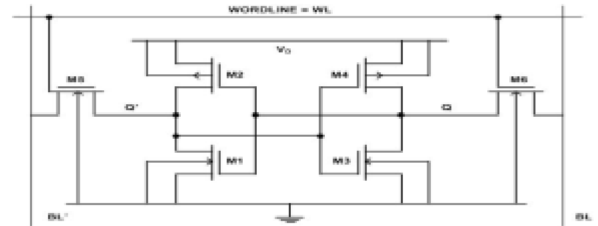


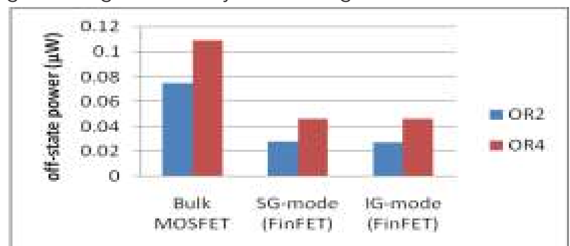
Fig. 7 6-T SRAM

VII. SIMULATION RESULTS

Simulations were carried out with SPICE tool using PTM for 45 nm FinFET and MOSFET technologies. Simulations are conducted with supply voltage, temperature and frequency of 1V, 70° C and 1 GHz respectively.

Fig. 8 shows off-state power, on-state power and delay of OR2, OR4 implemented using MOSFET and FinFETs. Implementation of SG and IG (single gate) modes of FinFETs outperforms MOSFET in all parameters. FinFET has negligible depletion and junction capacitance, which reduce the effective gate capacitance. Back gate creates inversion region faster and generates higher current capability to increase I_{ON}. Lower parasitic capacitance and higher I_{ON} provide significant improvement in delay and off-state power.

In SG-mode, two gates are strongly coupled to each other thereby lowering V_T as compared to IG-mode to achieve better delay performance as seen in Table 4. However, on-state and off-state power are reduced in IG-mode implementation compared to SG- mode. Reduced C_{ox} between two gates of IG-mode helps to reduce on-state power and dynamic V_T tuning reduces off-state power. Table 3 demonstrates performance comparison of domino OR8 logic implemented using MOSFET and FinFETs. FinFETs implementation (0.66V noise) shows significant reduction in on-state power and delay as compared to MOSFET due to (i) reduced clock and load capacitance that reduces total parasitic (ii) dynamic V_T tuning causing reduction in contention. Table 4 demonstrates relative improvement in gates using static and dynamic configurations.



(a) Off-State Power

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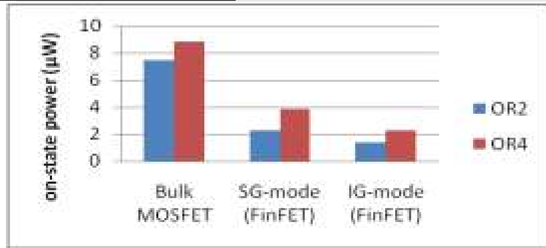
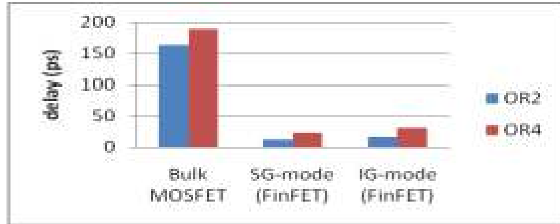


(b) On-State Power



(c) Delay

Fig. 8 Performance comparison of MOSFETs and FinFETs Implementations

TABLE 3 COMPARISON FOR Or8

Parameters	MOSFET	IG-mode (FinFET)
off-state power (μw)	0.423	0.397
on-state power (μw)	17.57	6.8
delay (ps)	289.6	25.63

TABLE 4 RELETIVE IMPROVEMENT IN GATES

Circuit configurations	Off-state power	On-state power	Delay
Static	≥ 236.95%	≥ 375.22%	≥ 598.70%
Dynamic	7%	262%	744.33%

Table 5 shows comparison of 6-T SRAM cell implemented using MOSFET and FinFET. FinFET implementation outperforms in terms of SNM, on-state and off-state power. However, such improvement is achieved at the cost of delay.

TABLE 5 COMPARISON OF 6-T SRAM CELL

Parameters	MOSFET	FinFET(IG)
SNM(mv)	250	344
off-state power(μw)	6.20	2.02
on-state power(μw)	674	276
delay(ps)	58.2	65.4

VIII. CONCLUSION

In order to study the merits of FinFETs, we examined the performance in various digital systems with reference to MOSFET implementation. FinFET outperformed MOSFET in terms of power and delay for static and dynamic circuit configurations. FinFET based memory configuration offered significant improvement in power and noise immunity with marginal impact on delay.

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