Standard 6T SRAM Bitcell

Electronics Engineering

KEYWORDS: Static Noise Margin (SNM), Bit cell, world line, data line,

Ajeet Singh	VITS Ghaziabad.
Sandeep Sharma	DIT University, Dehradun
Sanjay Kumar Singh	IPEC, Ghaziabad,
B K Singh	SIT Almorha

ABSTRACT

- In the recent past there has been substantial efforts were made to understand and model the stability of an SRAM bitcell. Many analytical models have been developed for the static noise margin (SNM) of an SRAM bitcell to optimize the bitcell design, to predict the effect of parameter variations on the SNM and to access the impact of intrinsic parameter variations on the SRAM bitcell stability. Some of the recent methods for measurement of SRAM stability are N-curve and bitline measurement techniques are discussed in this paper.

INTRODUCTION

A standard 6T SRAM bit cell consists of two identical CMOS inverters (INV-1 and INV-2) connected in a positive feedback loop. It forms a latch to store one-bit of information, either '1' or '0'. The internal nodes (Q and QB) of the bit cell always contain complementary values, as shown in Fig.1. The cross coupled inverter pair itself consists of two PMOS pull-up devices (M3 and M5) and two NMOS pull-down devices (M4 and M6). Two NMOS pass-gate (M1 and M2), which are controlled by the word line (WL), serve as switches between the inverter pair and the complementary pair of bit lines (BL, BLB) also called data lines, used to read in or write to the bit cell, as shown in Fig.1. The data in SRAM bit cell is stored as long as the power is maintained to the bit cell. The cross coupled inverter pair can be in one of the two stable states of an SRAM bit cell, which corresponds to the data stored '1' and '0', as shown in Fig. 2,a,b, respectively. The basic operations of a bit cell as a storage device are reading or writing new data to the bit cell. The read and write operations in a standard 6T SRAM bit cell are performed in the following ways.

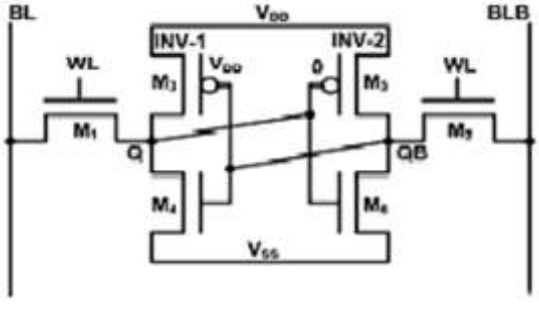

Fig.1. A Standard 6T SRAM Schmatic Diagram

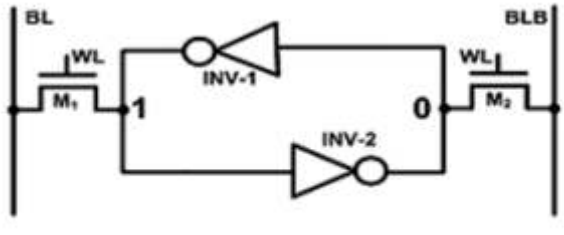

Fig. 2a. SRAM bit cell '1' stored

Read Operation

Initially, it is assumed that the internal data storage nodes Q and QB are at '0' and '1', respectively, which correspond to Fig. 2b.

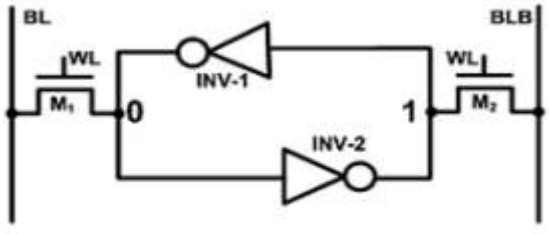

Fig.2b. SRAM bitcell '0' stored

To read a bit cell, the bit lines (BL and BLB) are pre- charged to the supply voltage (VDD). When, the word line (WL) is asserted to high and rise from '0' to '1', result, one of the bit cell sides (node) stores the logical '0'; that side of the bit line is discharged through the pass-gate and pull down transistors. In standard 6T, as shown in Fig.1, devices M1 and M4 discharges the pre-charged bit lines BL. If BLB discharges, then the bit cell holds a logic '1' value, which correspond to Fig. 2a. If BL discharges, then the bit cell holds a logic '0' value, which correspond to Fig.2b. Depending upon whether the bit line BL or BLB is discharged, the bit cell is read as a logical '1' or '0'. A sense amplifier converts the differential signal exists on BL and BLB to a logic-level output.

De-assertion of the word line (WL) back to 0. During a read operation, the internal node (Q) of the bit cell that holds a logical '0' will pull its bit line (BL) low through the pass-gate transistor, M1 and pull down transistor, M4. It is important that the low internal node (Q) should not rise above the trip-point (switching threshold voltage) of the inverter INV-2, as shown in Fig. 1, to avoid a destructive read operation. A destructive read operation can be prevented by ensuring a large enough bit cell ratio (β), in other words, pull-down transistors (M4 and M6) must be stronger than the access transistors (M1 and M2).

For a symmetric bit cell, bit cell ratio (β) is defined as [1]:

$$\beta = \frac{W_4/L_4}{W_1/L_1} = \frac{W_6/L_6}{W_2/L_2} \qquad (2.1)$$

Generally, the bit cell ratio can be varied from 1.25 to 2.5 depending on the target application and desired static noise margin (SNM) [1]. A larger bit cell ratio makes the bit cell robust and provides higher SNM and read current I_{read} (speed), at the expense of increased silicon overhead and leakage current. A smaller bit cell ratio, whilst maintaining an adequate speed and noise margin, makes the bit cell compact for a high density cache design but more vulnerable to process variation induced failures.

Read SNM Measurement

The best measure to quantify the stability of an SRAM bit cell during the read cycle and in hold state is the Static Noise Margin (SNM). The SNM is defined as the maximum amount of DC noise (VN) that can be tolerated by the cross-coupled inverter pair such that the bit cell retains its data [2]. The read SNM is extracted from the read voltage transfer characteristics (VTC). The read VTC can be measured by sweeping the voltage at the data storage node Q (or QB) with both bit lines (BL, BLB) and word line (WL) biased at VDD while monitoring the node voltage at QB (or Q).

Write Operation

The write operation or flipping the bit cell contents when initially assuming that the internal data storage nodes Q and QB are at '0' and '1', respectively, as shown in Fig.2b. Initially, word line (WL) = 0 and Pre-charge the bit lines (BL and BLB) to the supply voltage (VDD). After pre-charge, both the bit lines (BL and BLB) are disconnected from the supply voltage VDD). Then, Word line (WL) is activated to high (data enters the bit cell during this step), which, Place the data value on the BL and the complementary data value on BLB. The bit line BLB connected to the data storage node QB via M2 is driven to the ground potential by a write driver through the M2 pass-gate transistor, while the BL is remained held at VDD to pull node Q to high via M1 pass-gate transistor. As node Q and QB flip their states de-assert the word line (WL) back to 0. As a result, node QB pulled well below the trip-point of the INV-1, as shown in Fig.1, so that, the feedback loop in the cross-coupled inverter starts to work and the bit cell is flipped. It is important that a successful write operation primarily depends upon the properly sized pass-gate transistors and pull-up transistors. Hence, the pull-up ratio (PR) for a symmetric SRAM bit cell is defined as [1]:

$$PR = \frac{W_3/L_3}{W_1/L_1} = \frac{W_5/L_5}{W_2/L_2} \qquad (2.2)$$

During write operation fight occurs between pass-gate transistors (M1 and M2) and pull-up transistors (M3 and M5) mainly when the value of the data to be written into the bit cell is the opposite of the value that is currently stored in the bit cell. For instance, assumed that the bit cell currently holds a logic '1' and it is intended to write a logic '0' into the bit cell. Then, the situation correspond the following biasing conditions; BLB, WL and bit cell supply voltage is biased at VDD and BL is biased at VSS in Fig.2a. For a successful write operation, node QB must be pulled above the trip point of the inverter "INV1" and node Q must be pulled down below the trip-point of the inverter "INV2". In this mode, fight occurs between M1 and M3. Since M1 will try to bring node Q to down while M3 will try to keep node Q to high. Therefore, M1 must win the fight for a successful write operation. Once an inverter switches, it creates a self-reinforcing positive feedback action that continue until the bit cell has been fully placed into a new stable state.

A successful write operation can be guaranteed by choosing a lower PR value (generally, PR = 1), that can be achieved by employing the wider or stronger pass gate transistors (M1 and M2) instead of pull-up transistors (M3 and M5). However, increasing the width of the pass-gate transistors threatens the stability of the bit cell during the read cycle, or in other words reduces the read SNM of the bit cell.

Write SNM Measurement

Fig.3 shows the experimental set-up for measurement of write static noise margin (WSNM). During write operation M1 (or M3) and M5 (or M6) form a resistive voltage divider for the falling BL (or BLB) and storage node Q (or QB). If the voltage divider pulls Q below the trip-point of inverter 2 (INV-2), a successful write operation occurs. The write-ability of a SRAM bit cell can be gauged by the write SNM [3, 4]. The write SNM is extracted by a combination of read voltage transfer characteristics (VTC) and the write VTC. The read VTC is measured by sweeping the voltage at the storage node QB while monitoring the node voltage at Q. The write VTC is measured by sweeping the voltage at the storage node Q with BL and WL biased at VDD and BLB is biased at VSS while monitoring the voltage at node QB. The WSNM can be quantified by the side of the smallest square fitted inside the read and write VTCs. When WSNM fall negative, the read VTC and write VTC intersects each other suggesting the inability to write into the SRAM bit cell. The write-ability of an SRAM bit cell can also be characterized by the write trip point- voltage, which is defined as the maximum amount of voltage needed on the bit line to flip the bit cell content [5, 6]. The Write Static Noise Margin (WSNM) is measured through the write-trip point defined as the difference between VDD and the maximum bit line voltage required to flip the data storage nodes Q and QB.

Other SRAM Bit cell Stability Metrics

Some of the recent methods for measurement of SRAM stability are N-curve and bit line measurement techniques. SRAM stability metrics can broadly be classified into two categories: static and dynamic. In static SRAM stability metrics, a DC voltage is applied or swapped to estimate how much DC noise an SRAM bit cell can tolerate. The static stability metrics are further divided into two categories: conventional and large scale metrics.

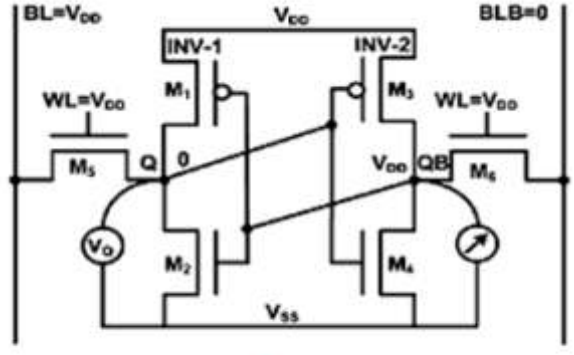

Fig.3. Experimental set-up for extracting the write statice noise margin

Conventional metrics are based on butterfly curves and N-curves. These metrics require access of internal nodes of an SRAM bit cell for measurement of stability and provides limited data for stability analysis. Access of internal nodes of all the SRAM bit cells is not feasible because of metal spacing constraints and area overhead associated to provide switch array. On the other hand, large scale metrics do not require access of internal data storage nodes for stability analysis; therefore, these metrics are suitable for dense large scale SRAM designs. In theses metrics, measurement of stability is done by accessing the bit lines (BL or BLB), word line (WL), and bit cell supply (VCELL).

N-Curve Stability Metrics

Fig. 4 [1] shows the experimental setup for extracting the N-curve of a standard 6T SRAM bit cell. The same setup can also be extended for other SRAM bit cell topologies. At the beginning of read access both bit lines (BL and BLB) are pre-charged to '1' and word line is activated to '1'. It is assumed that the internal storage nodes QB and Q are at '1' and '0', respectively. A voltage sweep Vin from 0 to VDD is applied at

the node Q and corresponding current supplied by the sweep voltage source Vin is measured as Iin.

The resulting relationship is plotted between Vin on x-axis and Iin on y-axis is called the N-curve, contains information for both read stability and write stability. There is no need of mathematical manipulation on the measured data as N-curve directly provides the functional information of SRAM bit cell. N-curve contains information for both voltage and current. Thus, allowing a complete functional analysis of the SRAM bit cell stability for both read and write operations with only one N-curve. However, major limitations of the N-curve based stability analysis is that it also requires the access of internal nodes of the SRAM bit cell similar to butterfly curves.

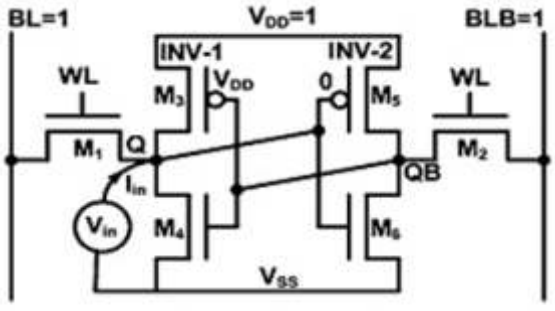

Fig.4. Experimental set up for extracting the N-curve of a standard 6T SRAM bitcell

Static Voltage and Current Metrics

The stability metrics derived from the N-curve are based on the combined voltage and current information for a SRAM bit cell. It shows static voltage noise margin (SVNM), static current noise margin (SINM), write trip voltage (WTV), and write trip current (WTI). The SVNM is defined as a maximum tolerable DC noise voltage at internal nodes of the bit cell before its content flips. Similarly, SINM can be defined as a maximum tolerable DC noise current injected at internal nodes of the bit cell before its content changes and it is measured as a peak current. These two metrics SVNM and SINM are used to characterize the bit cell read stability.

However, bit cell's write stability can be characterize the with the help of WTV and WTI. For this purpose N-curve has to be analyzed from right to left because for write operation, pulling down of precharged bit line (BLB) to ground so that the internal node QB get discharges. The WTV is the minimum voltage drop needed to change the internal nodes of the bit cell. The WTI is defined as a minimum amount of the current needed to write the bit cell which can be measured as a negative current peak.

Power Metrics

The N-curve is also used to derive the power metrics which includes both the voltage and current information for read stability and write stability. So, instead of using four metrics obtained from N-curve to analyze the stability of an SRAM bit cell, it would be easy to combine them in two power metrics, static power noise margin (SPNM) and write trip power (WTP) [7]. The SPNM is used to characterize the read stability. The SPNM is defined as the maximum tolerable DC noise power by the internal data storage nodes of the bit cell before its content changes.

The WTP characterizes the write stability of a bit cell and also defined as the minimum amount of power required to flip the data storage nodes.

Bit line Measurement Design Metrics

The conventional DC read and write static noise margin (SNM) metrics have some major drawbacks such as inability to measure them in dense functional SRAM arrays due to metal spacing constraints and area overhead associated to provide switch array. As a result, it produces inadequate number of data points for failure analysis of large size cache memories. In bit line measurement, SRAM read and write stability is characterized by accessing only the bit lines, word line, and the bit cell supply voltages [12]. It increases the number of line measurement can be used for analyzing the functional stability of an SRAM bit cell for read and write operations. In contrast to butterfly curve based stability analysis, bit line measurement directly provides the functional stability without mathematically manipulating the measured data. Bit line measurement can also be applied to detect and isolate the faulty SRAM bit cells in cache memory array [13].

Read Stability Measurement

Following characteristics can be used to measure read ability Measurement

Supply Read Retention Voltage (SRRV)

The read stability of an SRAM array can also be measured in terms of SRRV. For read stability measurement, both bit lines (BL and BLB) are kept floating around VDD while the word line (WL) is driven high, and the bit cell state is retained by keeping the bit cell supply sufficiently high. Therefore, SRAM bit cell read stability in functional SRAM array can be gauged by the minimum bit cell supply needed for data retention during read operation, which is referred as the supply read retention voltage (SRRV).

The SRRV of an SRAM bit cell can be defined as the difference between VDD and the value of the VCELL causing IBL to suddenly drop. Initially, when VCELL = VDD (i.e. SRRV = 0), the SRAM bit cell is biased for a nominal read operation with BL, BLB, WL and VCELL all are biased at VDD. If the SRRV is greater than zero, it indicates that bit cell supply voltage (VCELL) can be dropped below VDD without disturbing the bit cell state. Therefore, SRRV represents the maximum tolerable DC noise voltage at the bit cell supply before causing the destructive read operation.

Word line Read Retention Voltage (WRRV)

During read or write operation, word line is driven high causes read stress to SRAM bit cells having direct read access and all the unaccessed SRAM bit cells. This read stress can be further exacerbated by boosting the word line voltage above the VDD. Hence, the read stability of an SRAM bit cell can also be measured from the largest word line boost without flipping the bit cell contents, defined as word line read retention voltage (WRRV).

The WRRV of an SRAM bit cell can be defined as the difference between VDD and the boost in the word line voltage causing IBL to suddenly drop. Initially, when VWL = VDD (i.e. WRRV = 0), the SRAM bit cell is biased for a nominal read operation with BL, BLB, WL and VCELL all are biased at VDD. If the WRRV is greater than zero, it indicates that word line can be boosted above VDD without disturbing the bit cell state. Therefore, WRRV represents the maximum tolerable DC noise voltage at the word line before causing the destructive read operation.

Write ability Measurement

Following characteristics can be used to measure write ability Measurement.

Bit line Write Trip Voltage (BWTV)

The BWTV is quantified from the transfer characteristics of IBL versus VBLB, as the VBLB dropped low that causes the sudden fall in IBL. When BWTV is zero (BWTV = 0) the SRAM bit cell is biased for a nominal write operation. If the BWTV is greater than zero, it indicates that bit line voltage (VBLB) can be dropped below VDD for a successful write operation. Therefore, BWTV represents the maximum tolerable DC slack on the bit line to successfully write the bit cell.

Word line Write Trip Voltage (WWTV)

The WWTV is defined as the minimum word line voltage needed to

flip the bit cell content during a write cycle and it can be used to gauge the write ability of an SRAM bit cell in an SRAM array. The WWTV is quantified from the transfer characteristics of IBL versus the VWL voltage. The WWTV is defined as the difference of VDD and the VWL voltage which causes the sudden drop in the IBL. When WWTV = 0, the SRAM bit cell is biased for a nominal write operation with WL, BL and VCELL are biased at VDD and BLB is biased at VSS. If the WWTV is greater than zero, it indicates that word line voltage can be dropped below VDD for a successful write operation. Therefore, WWTV represents the maximum tolerable DC slack on the word line to successfully write the bit cell.

Dynamic Stability Analysis

It is well known that both SNM and WNM, in general, are not capable of capturing different effects such as coupling, charge sharing, transient, and other dynamic bit cell behavior under read and write operations. Therefore, dynamic stability analysis of a SRAM bit cell is must to determine the functionality or a successful read and write operation in time domain.

Dynamic Read Stability

Fig. 5 shows an SRAM bit cell under read access for different pulse widths TA and TB. It illustrates the importance of pulse width during read access and shows that how insufficient pulse width can lead to latch a wrong value. Fig.5 shows which bit lines are pre-charged to VDD before the read access cycle and word line is active high during read access. In Fig.5a, word line pulse width TA is too short, therefore, bit line capacitance is not discharged sufficiently to overcome the offset in the sense amplifier. As a result, wrong value is latched by the sense amplifier. Similarly, a successful read access operation is shown in Fig.5b for a word line pulse width TB. The word line pulse width TB is good enough to discharge the bit line (BL) and causes sufficient differential voltage to overcome the offset or trigger the sense amplifier. As a result, it latches the correct value of the data stored in the bit cell. It emphasize that there should be a critical word line pulse width, Taccess (TA < Taccess < TB), for which sense amplifier is on the threshold of a successful read access that is defined as the read access time. This is similar to dynamic read access failure defined in [19, 20, 21].

Dynamic Write Stability

Dynamic write failure of a standard 6T SRAM bit cell, as shown in Fig.6, can be studied under following biasing conditions that are correspond to a write operation. The bit line (BL) is charged to VDD and its complementary bit line (BLB) is tied to VSS and the word line (WL) is activated with different pulse widths (TA and TB). The word line pulse width TA is too short to overwrite the internal data storage nodes Q and QB of the SRAM bit cell. As a result, node Q and QB return back to their original states after the word line pulse TA is deasserted, as shown in Fig. 6b. It is corresponding to the write failure because bitcell's content are not changed during write access which is not desirable. The dynamic write failure, therefore, can be defined that if the voltage on the node initially storing '1' (QB) could not reach the trip point of the opposite inverter (INV1) during the wordline (WL) pulse then the bitcell will not successfully be written. In Fig. 6c, pulse width TB is sufficient to complete the write operation, that is, node Q and QB change their states before the deassertion of wordline pulse width TB. Therefore, there should be critical pulse width Twrite (TA < Twrite < TB), for which the bitcell is on threshold of a successful operation.

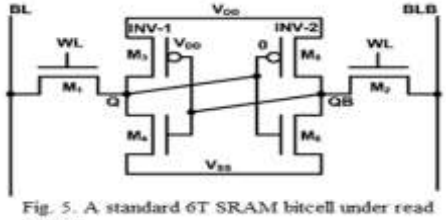

Fig. 5. A standard 6T SRAM bitcell under read access

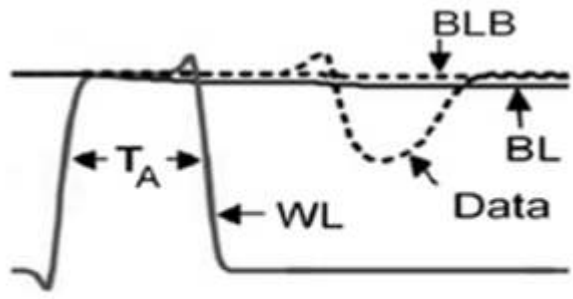

Fig. 5a. Read access with wordline pulse width, T_A

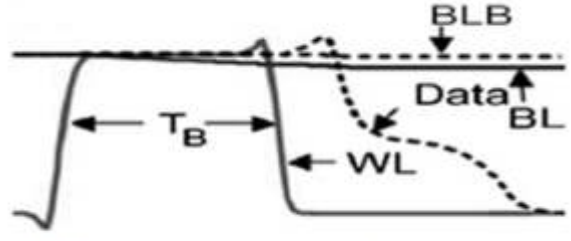

Fig. 5b. Read access with wordline pulse width T_B

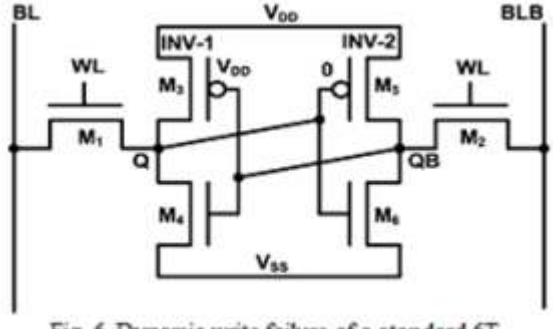

Fig. 6. Dynamic write failure of a standard 6T SRAM bitcell

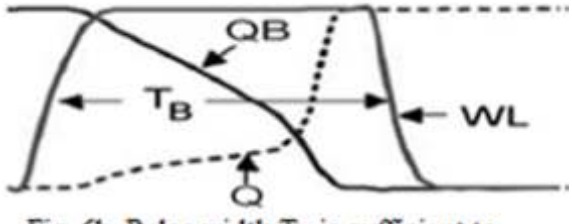

Fig. 6b. Pulse width T_B is sufficient to complete the write operation

Conclusion

The functionality of a SRAM bit cell can be ensured by analyzing different stability criterion; therefore, static and dynamic stability analysis techniques have been exhaustively studied and presented in a comprehensive manner. Limitations of static stability analysis techniques and how they are pessimistic and optimistically estimate the write and read SNM for failure analysis emphasize the need of dynamic stability analysis. For large size cache memories, where butterfly curve and N-curve approaches do not provide adequate number of data point for stability analysis, bitline measurement techniques play a significant role and provide large number of failure points for statistical analysis of stability are also presented. The

dynamic stability analysis approach for a successful read and write operations and the importance of word line pulse width are also explained.

REFERENCE

[1] Singh, J., Mohanty, Saraju P., Pradhan, Dhiraj K., (2013), "Robust SRAM Designs and Analysis", Springer Science+Business Media New York.|[2] Seevinck, E., List, F., Lohstroh, J., (1987), "Static-noise margin analysis of MOS SRAM cells", J.Solid-State Circuit 25(2), 784–754.|[3] Bhavnagarwala, A., Kosonocky, S., Radens, C., Stawiasz, K., Mann, R., Ye, Q., Chin, K., (2005), "Fluctuation limits amp; scaling opportunities for CMOS SRAM cells", In IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest, Washington, pp. 659–662. |[4] Bhavnagarwala, A., Kosonocky, S., Radens, C., Chan, Y., Stawiasz, K., Srinivasan, U.,Kowalczyk, S., Ziegler, M., (2008), " A sub-600-mv, fluctuation tolerant 65-nm CMOS SRAM array with dynamic cell biasing", IEEE J. Solid-State Circuit 43(4), 946–955.|[5] Jiajing W., Nalam, S., Calhoun, B.H., (2008), "Analyzing static and dynamic write margin for nanometer SRAMs, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)", 129–134.|[6] Heald, R., Wang, P., (2004) ,"Variability in sub-100 nm SRAM designs. In: International Conference on Computer Aided Design", 2004. ICCAD-2004, San Jose, pp. 347–352.|[7] Singh, J., Mathew, J., Pradhan, D., Mohanty,S., (2008), "Failure analysis for ultra low power NANO-CMOS SRAM under process variations", In IEEE International SoC Conference, 2008, pp. 251–254.|[8] Bhavnagarwala, A.J., Tang, X., Meindl, J.D., (2001), "The impact of intrinsic device fluctuations on CMOS SRAM cell stability", IEEE J. Solid-State Circuit 36, 658-665.[9] Agarwal, K., Nassif, S., (2006), "Statistical analysis of SRAM cell stability", In DAC '06: Proceedings of the 43rd Annual Conference on Design Automation, San Francisco, pp. 57–62. ACM Press, New York.|[10] Heald, R., Wang, P., (2004), "Variability in sub-100 nm SRAM designs", In IEEE/ACM International Conference on Computer Aided Design, San Jose, pp. 347–352. |[11] Takeda, K., Hagihara, Y., Aimoto, Y., Nomura, M., Nakazawa, Y., Ishii, T., Kobatake, H., (2006), " A read-static-noise-margin-free SRAM cell for low-vdd and high-speed applications", IEEE J. Solid-State Circuit 41(1), 113–121.|[12] Calhoun, B., Chandrakasan, A., (2006) ,"Static noise margin variation for sub-threshold SRAM in 65-nm CMOS", IEEE J. Solid-State Circuit 41(7), 1673–1679.|[13] Guo, Z., Carlson, A., Pang, L.T., Duong, K., Liu, T.J.K., Nikolic, B., (2009), "Large-scale SRAM variability characterization in 45 nm CMOS", IEEE J. Solid-State Circuit 44(11), 3174–3192.|[14] Wong, V., Lock, C., Siek, K., Tan, P., (2002), "Electrical analysis to fault isolate defect in 6T memory cells", In IEEE IPFA, pp. 101–104.|[15] Fischer, T., Amirante, E., Huber, P., Nirschl, T., Olbrich, A., Ostermayr, M., Schmitt-Landsiedel, D., (2008) " Analysis of read current and write trip voltage variability from a 1-MB SRAM test structure", IEEE Trans. Semicond. Manuf. 21(4), 534–541.|[16] Gierczynski, N., Borot, B., Planes, N., Brut, H., (2007), " A new combined methodology for write margin extraction of advanced SRAM". In IEEE International Conference on Microelectronic Test Structures 2007, ICMTS '07, pp. 97–100.|[17] Guo, Z., Carlson, A., Pang, L.T., Duong, K., Liu, T.J.K., Nikolic, B., (2008), "Large-scale read/write margin measurement in 45 nm CMOS SRAM arrays", In IEEE Symposium on VLSI Circuits, 2008, pp. 42–43.|[18] Heald, R., Wang, P., (2004), "Variability in sub-100 nm SRAM designs", In IEEE/ACM International Conference on Computer Aided Design, San Jose, pp. 347–352.|[19] Bhavnagarwala, A., Kosonocky, S., Radens, C., Stawiasz, K., Mann, R., Ye, Q., Chin, K., (2005), "Fluctuation limits amp; scaling opportunities for CMOS SRAM cells", In: IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest, Washington, pp. 659–662. |[20] Khalil, D., Khellah, M., Kim, N.S., Ismail, Y., Karnik, T., De, V., (2008), "Accurate estimation of SRAM dynamic stability", IEEE Trans. Very Large Scale Integr. Syst. 16(12), 1639–1647.|[21] Mukhopadhyay, S., Mahmoodi, H., Roy, K., (2005) , "Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS", IEEE Trans. Comput. Aided Des. Integr. Circuit Syst. 24(12), 1859–1880.|[22] Toh, S.O., Guo, Z., Liu, T.J.K., Nikolic, B., (2011), "Characterization of dynamic SRAM stability in 45 nm CMOS", IEEE J. Solid-State Circuit 46(11), 2702–2712.