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To compare the performance, process variability of Tri-Gate Bulk FINFET and SOI FINFET at nanoscale regime

Physics

KEYWORDS: Tri gate FINFET, Bulk, Silicon-On-Insulator, Short channel effect, DIBL, Subthreshold leakage (SL), Visual TCAD tool.

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ABSTRACT

The paper mainly deals with the comparison of bulk FINFET and SOI FINFET characteristics. The scaling tendency in device dimension require limit on short channel effect through the control of sub threshold leakage and DIBL characteristics. It can be achieved by proper device design. This paper also compares the performance improvement of Tri-gate Bulk and SOI FinFet. The simulation results are obtained with the help of Visual TCAD device simulator are well matched with the characteristics.

I. INTRODUCTION:

The scaling of CMOS transistors has finally reached the boundary at size of 22 nm. They frequently cite that CMOS transistors are approaching atomistic and quantum mechanical physical boundaries. Furthermore, the concern is not only about the incompleteness of the devices itself to continue operate steadily but also the impulsion from the economic and technology point of view. Silicon-based microelectronic devices have revolutionized our world in the past five decades. The need for higher computing speed and power at cheaper cost has increased by leaps and bounds in past several years. The Moore's Law holds even 50 years later and it has become more like a self-fulfilling prophecy. But now it reaches to its limits for the conventional MOSFET devices. So the New device structure was required to extend the Moore's law[1] . There are several important factors that could challenge CMOS from being used in future. We can divide these challenges into five different categories, specifically:

Physical challenges: As the device dimension reduces, increment of tunnelling and leakage currents also increases, which impacts the performance and functionality of CMOS devices[3].

Material challenges: These come from the inability of the dielectric material and wiring materials to provide reliable insulation to device and conduction, respectively with continued scaling.

Power-thermal challenges: As the density of Transistors ever increasing number of transistors integrated per unit-area also increases, which demands for larger power consumption and higher thermal dissipation.

Technological challenges: These are the results from the inability of lithography-based techniques to provide the resolution below the wavelength of the light to manufacture to CMOS devices.

Economic challenges: As the technology enhances the cost of production, fab, and testing that may reach a point where it will be not affordable from economic point of view.

SOI TECHNOLOGY:

With Silicon-On-Insulator (SOI) transistors are formed in thin layers of silicon that are not connected to the main substrate of the wafer and insulated by a layer of electrical insulator, usually silicon dioxide[2]. The thickness of silicon layer ranges from several microns to few nanometers for high-performance devices. The idea of isolating the active transistor from the rest of the silicon substrate reduces the electrical current leakage.

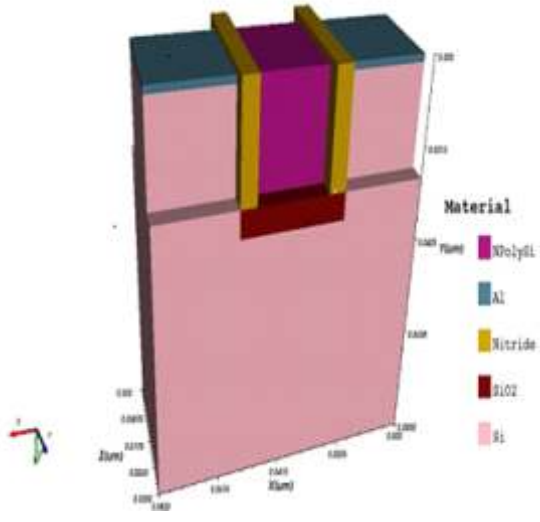

Fig1: Tri gate Bulk FINFET

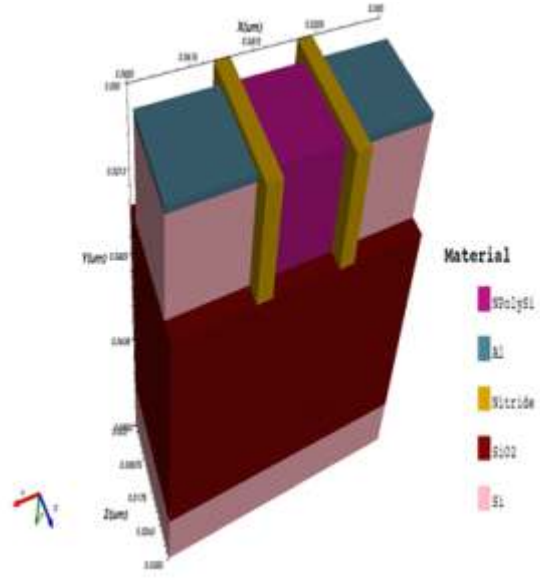

Fig2: Tri gate SOI FINFET

II.DEVICE SIMULATION AND RESULTS:

In this paper we have done simulation by using 3-D TCAD simulator COGENDA GENIUS. Table 1 which follows the device dimensions according to ITRS 2013 roadmap. For the simulation we have drift-diffusion, mobility, density-gradient quantum correction models being turned on. Enhanced Lombardi mobility model was activated which accounts for mobility degradation at si-sio2 interface. To find accurate threshold voltage constant current method is used.

Table1: Parameters used for simulations

Parameters	Value used
Top silicon width W_{Fin}	14nm
Silicon height H_{Fin}	20nm
Gate-oxide thickness	1nm
Gate work function	4.5ev
channel length	22nm
Source/drain doping	1e20 cm^{-3}
Channel doping	1e18 cm^{-3}

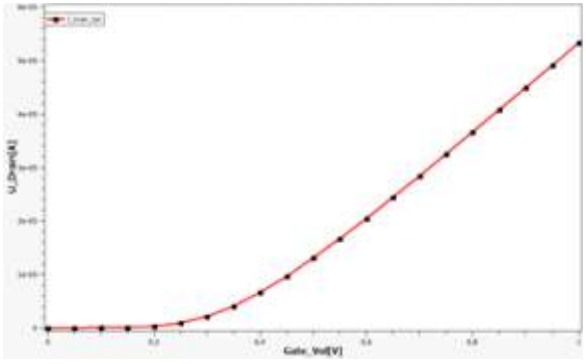

Figure 3: Constant Current Method implemented on the plot of I_D versus V_g Gate-voltage at which drain current exhibits 10e-7 Current is equal to threshold voltage of device. Here L=22nm, H=20nm, W=14nm, V_d=0.75V, Na=1E18, (Bulk FinFET)

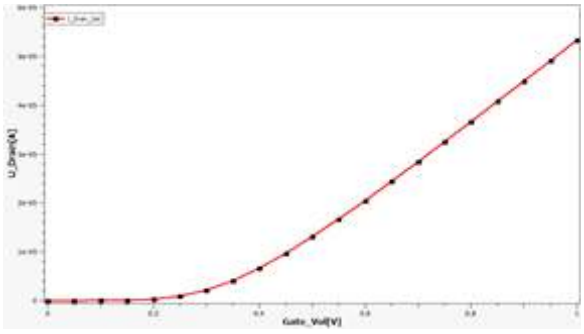

Figure 4: Constant Current Method implemented on the plot of I_D versus V_g Gate-voltage at which drain current exhibits 10e-7 Current is equal to threshold voltage of device. Here L=22nm, H=20nm, W=14nm, V_d=0.75V, Na=1E18, (Bulk FinFET)

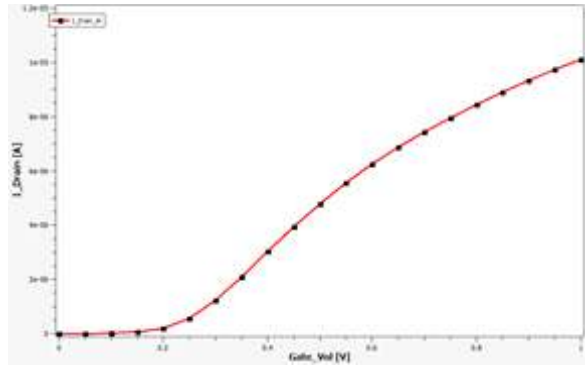

Figure 5: Constant Current Method implemented on the plot of $I_D$versus V_g Gate-voltage at which drain current exhibits 10e-7 Current is equal to threshold voltage of device. Here L=22nm, H=20nm, W=14nm, V_d=0.05V, Na=1E18, (SOI FinFET)

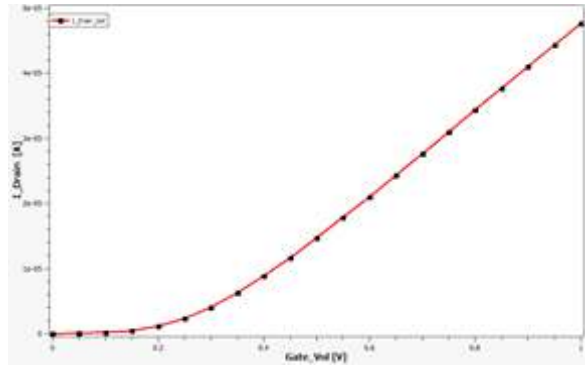

Figure 6: Constant Current Method implemented on the plot of $I_D$versus V_g Gate-voltage at which drain current exhibits 10e-7 Current is equal to threshold voltage of device. Here L=22nm, H=20nm, W=14nm, V_d=0.75V, Na=1E18, (SOI FinFET)

CONCLUSION:

This study describes the characteristics comparison of bulk FINFET and SOI FINFET. The scaling trend in device dimension require limit on short channel effect through the control of electrostatic parameters and DIBL characteristics .It can be achieved by proper device design

The performance characteristics of SOI FINFET and BULK FINFET[4] are compared. SOI-FinFET gives superior performance over bulk FinFET.

REFERENCE

[1] "Into The Nano Era" Moore's Law Beyond Planar Silicon CMOS by Howard R. Huff. | [2] "Impact of device parameters of triple gate soi-finfet on the performance of cmos inverter at 22nm" Prathima.A, Kiran Bailey ,K.S.Gurumurthy,Department of Electronics and Communication Engineering, BMSCE, Bangalore, Department of ECE,UVCE, Bangalore University ,Bangalore, International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.5, October 2012 | [3] "Performance comparison of bulk finfet with soi finfet in nano-scale regime" Sumanlata tripathi, ramanuj mishra, sandeep mishra, virendra pratap Yadav & r.a.mishra Department of Electronics & Comm. Engineering, MNNIT, Allahabad, India, International Journal of Electronics Signals and Systems (IJESS) ISSN: 2231- 5969, Vol-2, ISS-2,3,4, 2012 | [4] "SOI vs. Bulk FinFET: Body Doping and Corner Effects Influence on Device Characteristics" Mirko Poljak, Vladimir Jovanović, and Tomislav Suligoj, IEEE ,2008