

An EDDR Architecture for Motion Estimation Testing Applications



Engineering

KEYWORDS : motion estimation, error detection and data recovery, residue-and quotient code, design for testability, circuit under test.

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ABSTRACT

The critical role of motion estimation (ME) in a video coder, testing such a module is of priority concern. While focusing on the testing of ME in a video coding system, this work presents an error detection and data recovery (EDDR) design, based on the residue-and quotient (RQ) code, to embed into ME for video coding testing applications. An error in processing elements (PEs), i.e. key components of a ME, can be detected and recovered effectively by using the proposed EDDR design. Experimental results indicate that the proposed EDDR design for ME testing can detect errors and recover data with an acceptable area overhead and timing penalty. Importantly, the proposed EDDR design performs satisfactorily in terms of throughput and reliability for ME testing applications. While DFT approaches enhance the testability of circuits, advances in submicron technology and resulting increases in the complexity of electronic circuits and systems have meant that built-in self-test (BIST) schemes have rapidly become necessary in the digital world. BIST for the ME does not expensive test equipment, ultimately lowering test costs. Thus, extended schemes of BIST referred to as built-in self-diagnosis and built-in self-correction have been developed recently.

I. INTRODUCTION :

Advances in semiconductors, digital signal processing, and communication technologies have made multimedia applications more flexible and reliable. A good example is the H.264 video standard, also known as MPEG-4 Part 10 Advanced Video Coding, which is widely regarded as the next generation video compression standard. Video compression is necessary in a wide range of applications to reduce the total data amount required for transmitting or storing video data. Among the coding systems, a ME is of priority concern in exploiting the temporal redundancy between successive frames, yet also the most time consuming aspect of coding. Additionally, while performing up to 60%–90% of the computations encountered in the entire coding system, a ME is widely regarded as the most computationally intensive of a video coding system. A ME generally consists of PEs with a size of 4x4. However, accelerating the computation speed depends on a large PE array, especially in high-resolution devices with a large search range such as HDTV. Additionally, the visual quality and peak signal-to-noise ratio (PSNR) at a given bit rate are influenced if an error occurred in ME process. A testable design is thus increasingly important to ensure the reliability of numerous PEs in a ME. Moreover, although the advance of VLSI technologies facilitate the integration of a large number of PEs of a ME into a chip, the logic-per-pin ratio is subsequently increased, thus decreasing significantly the efficiency of logic testing on the chip. As a commercial chip, it is absolutely necessary for the ME to introduce design for testability (DFT). DFT focuses on increasing the ease of device testing, thus guaranteeing high reliability of a system. DFT methods rely on re-configuration of a circuit under test (CUT) to improve testability. While DFT approaches enhance the testability of circuits, advances in sub-micron technology and resulting increases in the complexity of electronic circuits and systems have meant that built-in self-test (BIST) schemes have rapidly become necessary in the digital world.

DISADVANTAGES OF EXISTING:

- Poor performance in terms of high accuracy design for real time applications in DCT core on FPGA implementation.
- Does not achieve in terms of implementation on CMOS technology DCT core.

ADVANTAGES OF PROPOSED:

- To fit for Real Time application in DCT Core.

II. PROPOSED SYSTEM

The conceptual view of the proposed EDDR scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) in Fig. utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine

whether the CUT has errors.

DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results. Importantly, an array-based computing structure, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDDR scheme to detect errors and recover the corresponding data.

ADVANTAGES IN PROPOSED SYSTEM

1. More reliability.
2. Less number of gate counts.

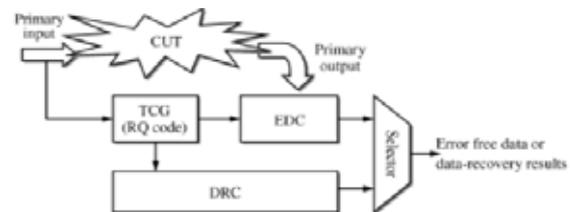


Fig.1. Proposed EDDR architecture

I. COMPRESSION

Wireless video transmission presents several problems to the design of a video coding system. First of all, some form of compression is needed for a bandwidth-limited system. Often, in a network environment for example, a certain amount of bandwidth is allocated to an individual user. Under these circumstances, a certain amount of "headroom" is allowed for each of the signal processing components based on user needs. The headroom for each of these components is usually not fixed, and is based on restricted channel capacity and networking protocols needed to service the needs of its users. Given this, and the fact that video requires the highest bandwidth in a multimedia environment, the ability to vary the compression rate in response to varying available bandwidth is desirable. To achieve a certain bandwidth requirement, some combination of the following is required:

Interframe compression: the idea behind inter frame compression is that consecutive frames tend to have a high degree of temporal redundancy, and that the difference frame between the two would have a large number of pixel values near zero. So the result is a much lower energy frame than the originals, and thus more amenable to compression. Figure 1-1 shows the strategy for interframe coding. Because of the complexity and power increase in implementing motion estimation for interframe coding (requiring more than 50% of the total number of computations per frame), the cost value is high for interframe coding. Algorithms using interframe coding are often termed video coding algorithm.

Intraframe compression: this implies spatial redundancy reduction, and is applied on a frame by frame basis. For situations where bandwidth is limited, this method allows for great flexibility in changing the compression to achieve a certain bandwidth. The key component in intraframe compression is the quantization, which is applied after an image transform. Because of the spatial correlation present after performing a transform (DCT or wavelet for example), quantization can be applied by distributing the bits based on visual importance of a spatially correlated image. This method of compression has the added advantage, that the compression can be easily varied based on available bandwidth on a frame by frame basis.

IV.METHODOLOGIES : Coding approaches such as parity code, Berger code, and residue code have been considered for design applications to detect circuit errors. Residue code is generally separable arithmetic codes by estimating a residue for data and appending it to data. Error detection logic for operations is typically derived by a separate residue code, making the detection logic is simple and easily implemented. For instance, assume that N denotes an integer, N_1 and N_2 represent data words, and m refers to the modulus. A separate residue code of interest is one in which N is coded as a pair: $N \cdot m$ is the residue N of m modulo . Error detection logic for operations is typically derived using a separate residue code such that detection logic is simply and easily implemented. However, only a bit error can be detected based on the residue code. Additionally, an error cannot be recovered effectively by using the residue codes. Therefore, this work presents a quotient code, which is derived from the residue code, to assist the residue code in detecting multiple errors and recovering errors. In order to simplify the complexity of circuit design, the implementation of the module is generally dependent on the addition operation. Additionally, based on the concept of residue code, the following definitions shown can be applied to generate the RQ code for circuit design. The corresponding circuit design of the RQCG is easily realized by using the simple adders (ADDS). Namely, the RQ code can be generated with a low complexity and little hardware cost.

V.DATA RECOVERY CIRCUIT

In this module will be generate error free output by quotient multiply with constant value (64) and add with reminder code. During data recovery, the circuit DRC plays a significant role in recovering RQ code from TCG. Notably, the proposed EDDR design executes the error detection and data recovery operations simultaneously. Additionally, error-free data from the tested PE_i or data recovery that results from DRC is selected by a multiplexer (MUX) to pass to the next specific PE_{i+1} for subsequent testing. Error concealment in video is intended to recover the loss due to channel noise, e.g., bit-errors in a noisy channel and cell-loss in an ATM network, by utilizing available picture information. The error concealment techniques can be categorized into two classes according to the roles that the encoder and the decoder play in the underlying approaches. Forward error concealment includes methods that add redundancy in the source to enhance error resilience of the coded bit streams. For example, I-picture motion vectors were introduced in MPEG-4 to improve the error concealment. However, a syntax change is required in this scheme. In contrast to this approach, error concealment by post-processing refers to operations at the decoder to recover the damaged images based on image and video characteristics.

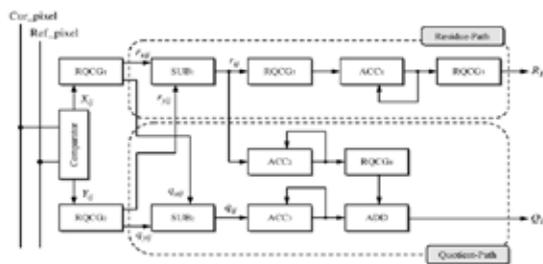
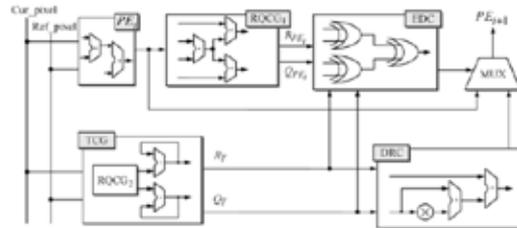


Fig. 2. Circuit design of the TCG

VI. ERROR DETECTION ARCHITECTURE

Our proposed EDDR scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results.



Applications : • The popularity of MP3 audio has established a massive installed base of hardware that can play back MPEG-1 Audio (all three layers).

- “Virtually all digital audio devices” can play back MPEG-1 Audio.[41] Many millions have been sold to-date.
- Before MPEG-2 became widespread, many digital satellite/cable TV services used MPEG-1 exclusively.
- The widespread popularity of MPEG-2 with broadcasters means MPEG-1 is playable by most digital cable and satellite set-top boxes, and digital disc and tape players, due to backwards compatibility.
- MPEG-1 is the exclusive video and audio format used on Video CD (VCD), the first consumer digital video format, and still a very popular format around the world.
- The international Digital Audio Broadcasting (DAB) standard uses MPEG-1 Layer II audio exclusively, due to MP2’s especially high quality, modest decoder performance requirements, and tolerance of errors.

VIII. CONCLUSIONS

This paper presents an FPGA implementation of efficient architecture for computing the 2-D DCT with distributed arithmetic. The proposed architecture requires less hardware than conventional architectures which use the original DCT algorithm or the even-odd frequency decomposition method. The modules of the transpose memory and parallel Distributed Arithmetic 2-D DCT architecture were designed and synthesized. The paper contributed with specific simplifications in the multiplier stage, by using shift and adds method, which lead to hardware simplification and speed up over architecture.

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