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Fpga Implementation of low Power Multi Channel Generalized Pid Controller Frame Work for Industrial Automation Applications

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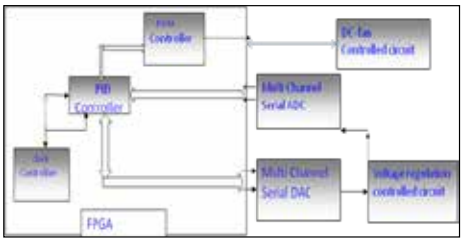
ABSTRACT

Proportional-Integral-Derivative (PID) controllers are universal control structure and have widely used in automation systems, they are usually implemented either in hardware using analog components or in software using Computer-based systems. In this work, we focused our works on building a multi-channel PID controller by Field Programmable Gate Arrays (FPGAs). Combining FPGA with high speed multi-channel serial ADC and serial DAC, the designed system has the effects of fast speed, high accuracy, compact size and cost effectiveness. To overcome the hardware complexity by the use of more processors for multi channel, we are using single pid controller for multi channel .Multi channel can be implemented by the use of FPGA.when the error is more it can DIFFERENTIATE and produce the constant output, when signal is low when compared to reference signal it can INTEGRATE it.FPGA can offer parallel processing, more speed.

I.INTRODUCTION

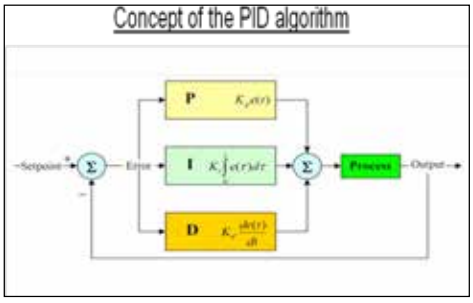
The modern digital control systems require more and more strong and fastest calculation components. This type of elements becomes indispensable with the utilization of some new control algorithms like the fuzzy control, the adaptive control, the sliding mode control, and so on. However, most of the abovementioned control structures need the system model, or some training data, to determine the controller's parameters. To consider the industrial application, although PID controllers are the oldest type, it is still the most important one to attain the desired control performance for its simple control structure and easily parameter tuning. Thus, regarding the design of universal control structure, PID controller is the most commonly used one. During the past years, FPGA applications in mechatronics, control and signal
Processing have been growing in relevance as an
Economic and reliable option made to fulfill the requirements of critical processes

Block diagram of Multi channel PID controller implementation FPGA



II. PID CONTROLLER:

A proportional–integral–derivative controller (PID controller) is a generic control loop feedback mechanism (controller) widely used in industrial control systems – a PID is the most commonly used feedback controller. A PID controller calculates an "error" value as the difference between a measured process variable and a desired set point. The controller attempts to minimize the error by adjusting the process control inputs.



The PID controller is named after its three correcting terms, whose sum constitutes the manipulated variable (MV). The proportional, integral, and derivative terms are summed to calculate the output of the PID controller. Defining u(t) as the controller output, the final form of the PID algorithm is:

$$u(t) = MV(t) = K_p e(t) + K_i \int_0^t e(\tau)\,d\tau + K_d \frac{d}{dt} e(t)$$

Where
Pout: Proportional term of output
Kp: Proportional gain, a tuning parameter
Ki: Integral gain, a tuning parameter
Kd: Derivative gain, a tuning parameter
e: Error = SP − PV
t: Time or instantaneous time (the present)

A) Proportional term:

The proportional term makes a change to the output that is proportional to the current error value. The proportional response can be adjusted by multiplying the error by a constant Kp, called the proportional gain.

The proportional term is given by:

$$P_{out} = K_p e(t)$$

A high proportional gain results in a large change in the output for a given change in the error. If the proportional gain is too high, the system can become unstable. In contrast, a small gain results in a small output response to a large input error, and a less responsive or less sensitive controller. If the proportional gain is too low, the control action may be too small when responding to system disturbances. Tuning theory and industrial practice indicate that the proportional term should contribute the bulk of the output change.

B) Integral term:

The contribution from the integral term is proportional to both the magnitude of the error and the duration of the error. The integral in a PID controller is the sum of the instantaneous error over time and gives the accumulated offset that should have been corrected previously. The accumulated error is then multiplied by the integral gain (Ki) and added to the controller output.
The integral term is given by:

$$I_{out} = K_i \int_0^t e(\tau)\,d\tau$$

The integral term accelerates the movement of the process towards set point and eliminates the residual steady-state error that occurs with a pure proportional controller. However, since the integral term responds to accumulated errors from the past,

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it can cause the present value to overshoot the set point value.

C) Derivative term
The derivative of the process error is calculated by determining the slope of the error over time and multiplying this rate of change by the derivative gain Kd. The magnitude of the contribution of the derivative term to the overall control action is termed the derivative gain, Kd.

The derivative term is given by:

$$D_{\text{out}} = K_d \frac{d}{dt} e(t)$$

The derivative term slows the rate of change of the controller output. Derivative control is used to reduce the magnitude of the overshoot produced by the integral component and improve the combined controller-process stability. However, the derivative term slows the transient response of the controller. Also, differentiation of a signal amplifies noise and thus this term in the controller is highly sensitive to noise in the error term, and can cause a process to become unstable if the noise and the derivative gain are sufficiently large. Hence an approximation to a differentiator with a limited bandwidth is more commonly used. Such a circuit is known as a Phase-Lead compensator.

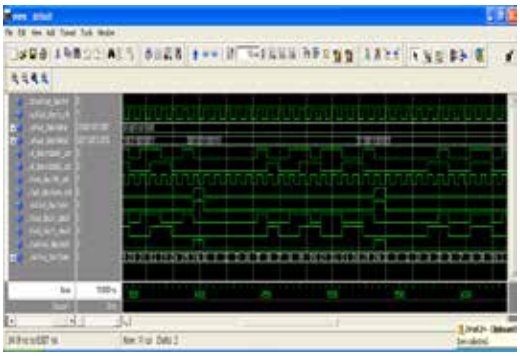
III. ADC MODULE:
FPGAs are well suited for serial Analog to Digital (A/D) converters. This is mainly because serial interface consumes less communication lines while the FPGA is fast enough to accommodate the high speed serial data. The ADCS7476MSPS is a high speed, low power, 12-bit A/D converter. Consumes 80 ns time for one cycle. A/D converter is a high speed serial interface that interfaces easily to FPGAs. The A/D interface adapter (AD1_PMOD) is implemented within the FPGA.

$$I_{\text{out}} = K_i \int_0^t e(\tau)\, d\tau$$

IV. DAC MODULE:
The DAC121S101 is a dual, 12-bit voltage out Digital to Analog (D/A) converter. This device uses a versatile 6-wire serial interface that operates at a clock up to 20 MHz The serial input register is 16 bits wide; 12 bits act as data bits for the D/A converter, It is interfaced to an FPGA as illustrated in Fig. 3. The D/A interface adapter (DAC_toplevel), which is implemented within the FPGA, facilitates parallel data input for the dual D/A converters

Chip Scope:
Chip Scope is embedded, software based logic analyzer. By inserting an "integrated controller core" (icon) and an "integrated logic analyzer" (ila) into your design and connecting them properly, you can monitor any or all of the signals in your design. Chip Scope provides you with a convenient software based interface for controlling the "integrated logic analyzer," including setting the triggering options and viewing the waveforms.

Simulation Waveform:



Waveform Description
Rst is used to reset the module or clear the privies data, clk is used for the synchronization, when the rising edge of clk is '1' then state is a counter goes on counting from '0' to '16'count's. if count is '15' then data present in data1 &2 will be forced on to the shift resister's (signal's), if count is above '3' then data in shift resister's will be forced on to output's from LSB to MSB till the count is '15' by shifting 1 bit for each count. Sync_out and pclk will be '1'when count is "15".

V.CONCLUSION
To overcome the hardware complexity by the use of more processors for multi channel, we are using single pid controller for multi channel .Multi channel can be implemented by the use of FPGA.when the error is more it can DIFFERENTIATE and produce the constant output, when signal is low when compared to reference signal it can INTEGRATE it.FPGA can offer parallel processing, more speed.

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