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Research Paper

Multi serial to Ethernet High Speed DATA Networks

Engineering

KEYWORDS : UART, LAN, CPU, MAX232, TCP/IP, Ethernet, Xilinx, FPGA, VHDL,

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ABSTRACT

The Multi serial Ethernet high speed data network programmable gate array (FPGA) with network interface chip is implemented in this project. The Ethernet send data as frame format after receiving serial data, indirectly achieves multi-serials communication, simplifies cabinet wiring and improves CPU's efficiency. In this project we use UARTS .Speed on Ethernet is limited to maximum 100 Mbps only In this net work provide without internet using LAN connection Various data will be captured by FPGA and will be sent on a serial line. read the data from these UARTS Receive and transform the data in it. On FPGA logic also will be implemented to read data from multiple numbers of serial ports. Write data in to memory location and transmitted data out put The WIZ Net module takes data from serial port and sends to PC in Ethernet form. In PC application will be developed to read data from Ethernet.

I. Introduction

Multi serial Ethernet data networks based on field programmable gate array (FPGA) communicate in UART mode[2]. In order to achieve multi-serials communication firstly, this paper introduced the structure and working principle of system. Then the design of system's hardware and software programming were described, as well analyzed configuration of every module and communication of serial ports Ethernet connectivity is achieved with small Ethernet adapter (serial to Ethernet) two serial ports of

UART was shown in Chips cope modules compared with traditional methods, it possesses the characters of high-integration, low-power, and flexibility

II. Structure And Working Principle

Ethernet module and level converter using a flexible FPGA programming feature, a UART can be designed in it. If several UARTs are in it, the system has the capacity of communication with multiple serial ports. The Ethernet module implements Ethernet communication and is configured at the time of initialization. main function is to achieve communication between

the serial devices and Ethernet When it receives data from devices, will choose useful data from serial data frame following the communication protocol, and send data after packaged. When

it receives data from Ethernet, it firstly unpacks the frame and determines the port number to transfer data to its buffer and adds the synchronous DATA.

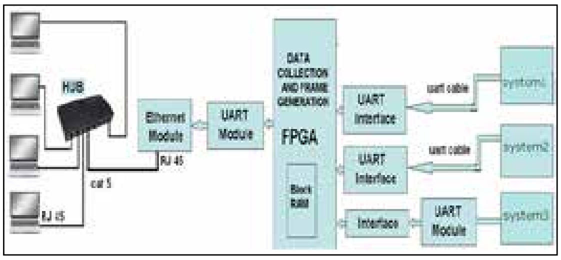

Fig.2.1 Top Level Block Diagram

III. Hardware Design

MAX232: The MAX232 is an integrated circuit that converts signals from an RS-232 serial port to signals suitable for use in TTL compatible digital logic circuits. The MAX232 is a dual driver/receiver and typically converts the RX, TX, CTS and RTS signals. The drivers provide RS-232 voltage level outputs (approx. ± 7.5 V) from a single + 5 V supply via on-chip charge pumps and external capacitors. This makes it useful for implementing RS-232 in devices that otherwise do not need any voltages outside the 0 V to + 5 V range, as power supply design does not need to be made more complicated just for driving the RS-232 in this case The receivers reduce RS-232 inputs (which may be as high as ± 25 V), to standard 5 V TTL levels. These receivers have a typical threshold of 1.3 V, and a typical hysteresis of 0.5 V. The later MAX232A is backwards compatible with the original MAX232 but may operate at higher baud rates and can use smaller external capacitors – 0.1 µF in place of the 1.0 µF capacitors used with the original device. The newer MAX3232 is also backwards compatible, but operates at a broader voltage range, from 3 to 5.5 V. Pin to pin compatible: ICL232, ST232, ADM232, HIN232

3.1UART BLOCK:

The UART is a serial interface with a frame format of start bit of active low '0'at beginning of frame and 8 bit of information with a stop bit of active high'1' signal at the end. The operation of UART is controlled by Clock signal which is fed from external crystal.

(a)UART Functions:

In addition to the basic job of converting data from parallel to serial for transmission and from serial to parallel on reception, a UART will usually provide additional circuits for signals that can be used to indicate the state of the transmission media, and to regulate the flow of data in the event that the remote device is not prepared to accept more data. For example, when the device connected to the UART is a modem, the modem may report the presence of a carrier on the phone line while the computer may be able to instruct the modem to reset itself or to not take calls by raising or lowering one more of these extra signals. The function of each of these additional signals is defined in the EIA RS232-C standard.

(b)UART Receiver:

This module is mainly responsible for data reception and the conversion of data. It mainly contains data registers and receivers. When the valid stop bit is detected, data are sent into the register. When the size equals to the setting value, data in the register are transferred into the I/O buffer. Receive controller mainly includes a counter and a 8 bits shift-register. It is controlled by the state machines.

(c)UART Transfer :

This module is used to send bus data received from Ethernet. It consists of transmitter and data registers. When the command is executed, transfer will send data in serial form until the send counter is 0, which means over. At last, the flag bit is set. The transmitter is a 8-bit shift register. As long as data register is not empty, shift register would constantly read data, add start and stop bits and send them in asynchronous frame format. It is also controlled by state machines When the send clock is high, if the data register is full, the data will sent in order. The coordinated communication of multiple serial ports: in order to allow ports communicate effectively, there is a need to administer them. As we know, the FPGA processing speed is far greater than peripheral transmit data rate, so once I/O buffer receives data from any serial port, the data can be read by Ethernet interface chip directly. So long as the serial data start address and end address doesn't conflict. When the send clock is high, if the data register is full, the data will sent in order. The coordinated communication of multiple serial ports: in order to allow ports communicate effectively, there is a need to administer them. As we know, the FPGA processing speed is far greater than peripheral transmit data rate, so once I/O buffer receives data from any serial port, the data can be read by Ethernet interface chip directly. So long as the serial data

UART receiver handles reception of data from RS232 port. Main functions of receiver block are to convert the serial data to parallel data, and check the correctness of data from parity and store the received data. UART receiver state machine. The receiver is in IDLE state by default. When the serial data pin goes low, indicating the start bit, the state machine enters DATA0 state. The data is received, one bit at a time from LSB to MSB in states DATA0 to DATA7.

If parity is enabled, the state machine checks the parity bit received against the parity obtained from received data. If the data received is fine, the (data_rx_done) bit is set to '1' and the receiver goes back to IDLE state again. .

(d) LAN :
LAN-based routers greatly extend the speed, distance, and intelligence of Ethernet LANs. Routers also allow traffic to travel along multiple paths. Routers, however, do require a common protocol between the router and end stations

IV. Simulation & Results

In this simulation, two ports are used to test the accuracy of receiving and transmitting, by using upper machine data analysis tools programmed in -Modelsim Xilinx Edition (MXE) The UARTs have worked correctly for a long time. Synthesis, P&R USING Xilinx ISE,On chip verificaiton Xilinx Chipscope Hardware Using Xilinx Spartan 3 Family FPGA

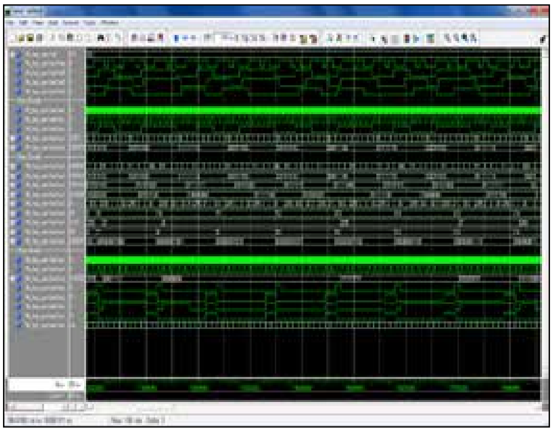

Fig. 4.1 Top Level - Modelsim Simulation Results

V. Conclusions

The communication between monitor computer and port devices, improve the efficiency of CPU, and ensure the processing of system in real time. FPGA's flexible programming features also allow further upgrade for system. Low cost, as the multi card solution can come in single FPGA card with small modules around it communicating local area no of systems trans faring the data on system to anther system Low power in comparison with multi card solution using Xilinx ISE 13.2 , Lot of scope for adding additional functionality on FPGA

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REFERENCE

[1] Ethernet h10032.www1.hp.com/ctg/Manual/bpe50027.pdf | [2] Moon Ho Lee, Alexander Dudin, Valentina Klimenok, Chang Joa Kim, "Multi-Server Queueing Model with Broadcasting Service, IEEE Communications Letters (11), pp 546-548, 2007. | [3] Shouqian Yu, Lili Yi, Weihai Chen, Zhaojin Wen, "Implementation of a Multi-channel UART Controller Based on FIFO Technique and FPGA," industrial Electronics and Applications, Harbin, China, May2007, pp. 2633-2638. | [4] Tong YAO, Yonghong YU, Lu Ding, "Fpga based for implementation of Multi-Serials to Ethernet Gateway", 978-1-4244-5874-5/10/$26.00 ©2010 IEEE | [5] Yu Zhang, Yugui Hu, Kuixi Yin, Jilian Li, "Implementation of Multiserials Expand Based on FPGA," Electronic Instrument, vol. 32, n. 1, 2009, pp. 233-236. | [6] F.S. Pan, F. ZHAO, J. Xi and Y. Luo, "Implement of Parallel Signal Processing Syttem Based on FPGA and Multi-DSP", Computer Engineering Vol 32, No. 23, Dec 2006, pp247-249 |