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Research Paper

Design and Implementation of Parallel Mac by Booth Algorithm

Engineering

KEYWORDS : Booth Multiplier, Modified Booth Algorithm (MBA), Carry Save Adder (CSA), Multiplier and Accumulator (MAC),

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ABSTRACT

The multiplier and multiplier - accumulator (MAC) are the essential elements of the digital signal processing such as filtering, convolution, and Inner products.In this paper, a new architecture of MAC for high-speed arithmetic has been designed. By combining multiplication with accumulation and devising a hybrid type of carry save adder (CSA), the performance was improved. Since the accumulator that has the largest delay in MAC was merged into CSA, the overall performance was elevated. The designed CSA uses 1's-complement based Modified Booth's Algorithm (MBA) and has the modified array for the sign extension in order to increase the bit density of the operandsThe New architecture of parallel MAC based on Modified Booth Algorithm is implemented using Verilog HDL (Hardware Description Language) and its functionality is verified through simulation using simulation software Xilinx-ISE 9.2i tool.

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations and a digital multiplier is the fundamental component in general-purpose microprocessors and digital signal processors. Multiplication-based operations such as Multiply-Accumulate and inner product are among some of the frequently used Computation-Intensive Arithmetic Functions (CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in many scientific and engineering applications. Since multiplication dominates the execution time of most DSP algorithms, there is a need of high speed multiplier. Typically, multipliers are implemented using the modified Booth algorithm (MBA), which requires modest hardware but results in unacceptably long delays. So, there were efforts to speed up MBA multipliers by using parallel implementations. For example, structures that merge the multiply and accumulate operations for use in several types of digital filters and filter banks are designed.

In general, a multiplier uses Booth's algorithm and array of full adders (FAs), i.e., the multiplier mainly consists of the three parts: Booth encoder, a tree to compress the partial products and final adder. The most effective way to increase the speed of a multiplier is to reduce the number of the partial products because multiplication proceeds with a series of additions for the partial products. To reduce the number of calculation steps for the partial products, MBA algorithm is applied mostly. To increase the speed of the MBA algorithm, many parallel multiplication architectures have been researched. Among them, one of the most advanced types of MAC for general-purpose digital signal processing has been proposed by Elguibaly.

In this paper, a new architecture for a high-speed MAC, in which computations of multiplication and accumulation are combined and a hybrid-type CSA structure is used to reduce the critical path and improve the output rate is designed. It uses MBA algorithm based on 1's complement number system. A modified array structure for the sign bits is used to increase the density of the operands. A carry look-ahead adder (CLA) is inserted in the CSA tree to reduce the number of bits in the final adder. In addition, in order to increase the output rate by optimizing the pipeline efficiency, intermediate calculation results are accumulated in the form of sum and carry instead of the final adder outputs.

II. OVERVIEW OF MAC

This section gives the basic operation of general MAC. Multiplication followed by accumulation is the operation of Multiplier - Accumulator (MAC) Unit. It consists of multiplying two values, then adding the result to the previously accumulated value,

which must then be restored in the registers for future accumulations. Fig. 1 shows the operational steps of basic MAC explicitly

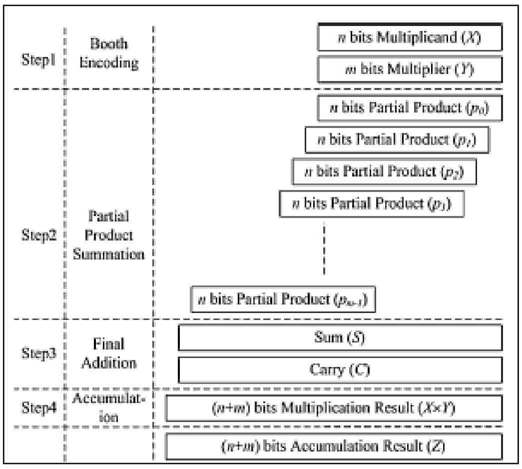

Fig. 1. Basic arithmetic steps of Parallel MAC

III. NEW MAC ARCHITECTURE

The new CSA architecture that complies with the operation of the new MAC is shown in the Fig. 5.

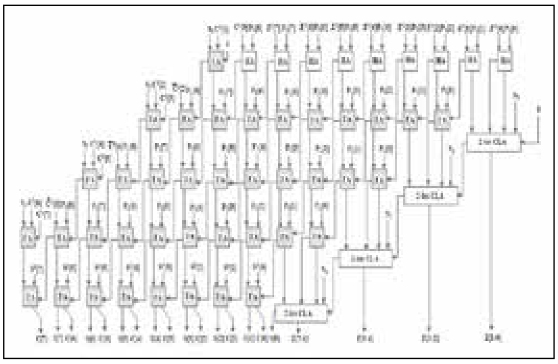

Fig. 5. CSA Architecture of the new 8 x 8-bit MAC arithmetic

In Fig. 5, Si is to simplify the sign expansion and Ni is to compensate 1's complement number into 2's complement number. S1[i] and C1[i] correspo CC o the ith bit of the feedback (previous) sum and carry and 1[i] corresponds to complement of C1[i]. S[i] and C[i] correspond to ith bit of present sum and carry output from CSA tree. Z[i] is the ith bit of the sum of the lower bits for each partial product that were added in advance and Z1[i] is the previous result. In addition, Pj[i] corresponds to the ith bit of the jth partial product. Since the multiplier is for 8 bits, totally four partial products (P0[7:0] ~ P3[7:0]) are generated from the Booth encoder. In (4.11), d0Y and dN/2-12N-2Y correspond to P0[7:0] and P3[7:0], respectively. This CSA requires at least four rows of FAs (full adders) for the four partial products. Thus, totally five FA rows are necessary since one more level of rows are needed for accumulation. For an n x n-bit MAC operation, the level of CSA is (n/2 + 1). The gray square in Figure 4.5 represents an FA and the white square is a half adder (HA). The rectangular symbol with five inputs is a 2-bit CLA with a carry input.

The critical path in this CSA is determined by the 2-bit CLA. It is also possible to use FAs to implement the CSA without CLA. However, if the lower bits of the previously generated partial

I. IMPLEMENTATION RESULTS

This section gives the simulation results for the new MAC implementation in Verilog HDL. The simulation has been done using Xilinx ISE. Fig. 6 shows the simulation results of 8x8bit MAC operation.

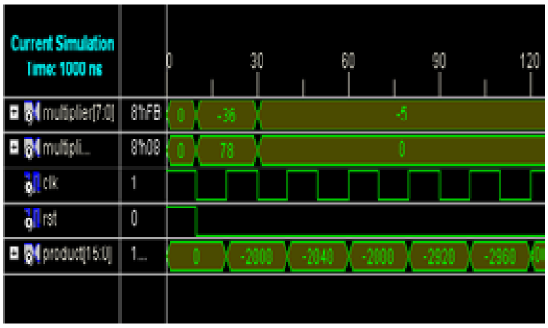

Fig. 6. Simulation result of 8 x 8-bit MAC

CONCLUSION

In this paper, a new architecture for MAC, the key operation for digital signal processing and multimedia information processing has been designed and implemented using Verilog HDL. This design of new architecture of MAC is based on 1's complement based Modified Booth Algorithm. This design adopts the modified array for addition of 2's complement numbers to eliminate the sign-extension so that the bit density of operands can be increased.

The accumulation is done using carry-save technique. Since accumulation is carried out using the result from step 2 instead of that from step 3, step 3 does not have to be run until the point at which the result for the final accumulation is needed. The overall performance of the proposed MAC is improved by eliminating the accumulator itself by combining it with the CSA function. This architecture has the smallest number of inputs to the final adder as compared with the previous architectures which increases the performance and the output rate.

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